Mitigating Non-linear DAC Glitches Using Dither in Closed-loop Nano-positioning Applications

Ahmad Faza', John Leth and Arnfinn A. Eielsen

***Abstract*— Digital-to-analog conversion is essential in digital signal processing applications, including closed-loop control schemes. Noise and distortion in digital-to-analog converters result in reduced performance for high-precision mechatronics such as nano-positioning. Glitches are common in practical switched systems such as digital-to-analog converters; observed as an output disturbance. Due to the wide-bandwidth, impulse-like behavior, control law bandwidth is generally too low to provide adequate attenuation; deteriorating open and closed-loop performance. This article demonstrates how large-amplitude high-frequency periodic dither mitigates the effect of glitches in a nano-positioning system under closed-loop control. Simulations are performed using a model that includes significant non-linearities with a response fitted to an off-the-shelf commercial device, as well as using standard linear time-invariant models for other system components fitted to the responses of common, commercially available devices. The results highlight the significance of reconstruction filter design when applying dithering in this setting.**

I. INTRODUCTION

A number of non-ideal effects arise in digital-to-analog converters (DACs). Fundamentally they introduce error due to repeated spectra and quantisation caused by time and value discretisation inherent to digital signal processing [1,2]. Non-ideal effects include element mismatch, thermal and semiconductor noise, and slew-rate limitations. Timing mismatches for transistor switching generate disturbances in the form of glitches [3]–[10]. Glitches can typically be seen when a DAC switches between two output levels. The combination of these effects deteriorates the quality of reconstructed actuation signals and reduces the tracking performance in both open and closed-loop. Many of the effects, such as element mismatch, which is a static non-linearity, will effectively be mitigated when operating in closed-loop. Glitches, however, will not be mitigated. This is due to their wide-bandwidth, impulse-like behavior, where most of the power in the disturbance is outside the bandwidth of the control law. Given the widespread use of DACs as an interfacing component for modern control schemes, it is desirable to minimise the errors introduced by common, commercially available DACs. In [11,12], dither-based approaches to improve the effective linearity of DACs were proposed, but only included static effects. Dynamic glitch modeling and model properties were investigated in [13]. By introducing a dither signal and averaging using a low-pass filter, it was shown that the glitch short-duration, large-amplitude impulse-like behavior could be converted to a long-duration, small-amplitude step-like disturbance. This indicates a reduction of the effective bandwidth of the disturbance, and hence that it may be possible to mitigate the residual disturbance using closed-loop control.

Dither is a well-known method for mitigation of static effects in DACs, including quantisation [14,15] and element mismatch [12]. Dynamic effects are also known to be mitigated in a similar fashion [16], and this effect has been demonstrated for glitches [13]. Dither is a high-frequency periodic or stochastic signal introduced into a system to modify its non-linear characteristics [17]–[20]. If sufficient averaging (low-pass filtering) is present on the output of the non-linear element, there is a smoothing effect on the non-linearity, typically making it less pronounced. An advantage of this method is that no specific knowledge of the non-linearity is needed in order to obtain improved performance. Specifically, dithering can easily be retrofitted to existing devices such as DACs with little effort.

A. Contribution

This paper demonstrates the effect of dithering a glitch non-linearity on a nano-positioning system and shows how large-amplitude, high-frequency periodic dither can achieve significant improvement in reference tracking performance. Previous investigations into the effect of dithering in closed-loop nano-positioning applications [11] only included static effects, such as quantisation and element mismatch [12]. This work extends the investigation to include dynamic effects, by utilising a DAC model that includes all significant, observed non-linearities, with parameters fitted to the measured response of an off-the-shelf commercial device. The DAC model corresponds closely to the actual physical device, including glitches, as validated in [13]. Linear time-invariant models for other system components are used, fitted to the measured frequency responses of common, commercially available devices. Here, the work suggests that proper tuning of dither amplitude in closed-loop in combination with the design of an output feedback control law can achieve further glitch mitigation improvement over what is reported in [13]. It is demonstrated that complete glitch mitigation is possible, i.e. the averaged glitch response appears as a constant offset that subsequently can be removed by integral action.

II. SYSTEM DESCRIPTION AND MODELING

A diagram of the modeled system is shown in Fig. 1. It consists of the standard devices necessary for implementing a digital control law: Reconstruction filter, amplifier, sensor, anti-aliasing filter, digital-to-analog converter (DAC), and

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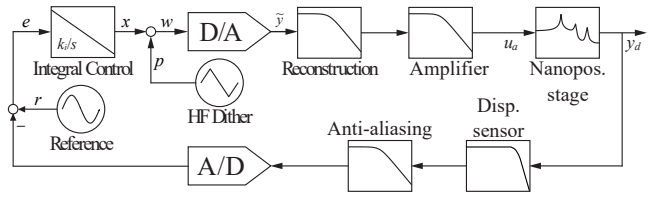

Fig. 1. System block diagram - r: reference position, e: tracking error, x: controlled state, p: periodic dither, w: DAC input, $\tilde{y}$: DAC output, u_a: actuation signal, y_d: plant displacement.

analog-to-digital converter (ADC). The ADC is assumed to be ideal. The objective is to achieve high-performance tracking control for the displacement y_d of a nano-positioning stage with piezoelectric actuators [21].

A. Modeling the DAC

1) Uniform quantisation: A DAC has 2^B levels, where B is the word size (bits). The quantisation step-size is

$$\delta = \frac{\Delta}{2^B - 1}\,, \tag{1}$$

where Δ is the physical output range of the DAC. A mid-tread uniform quantiser is defined using the truncation operator $T(w)$

$$k = T(w) = \left\lfloor \frac{w}{\delta} + \frac{1}{2} \right\rfloor\,, \tag{2}$$

where $\lfloor\cdot\rfloor$ denotes the floor operator and w the input which typically is dependent on time t, that is, $w = w(t)$. The truncation operator is a discontinuous function. The output y of the quantiser given an input w is

$$y = Q(w) = \delta T(w) = \delta k\,. \tag{3}$$

The quantisation error $q(w)$ is defined as the function

$$q(w) \triangleq y - w = Q(w) - w\,. \tag{4}$$

The output of the DAC can then be modeled as:

$$y = w + q(w)\,. \tag{5}$$

2) Modelling glitches: Glitches are transients generated when a digital-to-analog converter switches between two output levels. A glitch occurs when the analog signal value corresponding to a given digital code appears before or after the signal value of the previous code disappears at the DAC output. The glitch properties of a DAC are often specified by the net area of the glitch impulse response [22] or sometimes by the area at the worst-case code transition [23]. The glitch model proposed in [13], constructs glitches as short, symmetric or asymmetric rectangular pulses with unit areas driving a linear time-invariant (LTI) filter. The pulse response of the LTI filter can be designed to approximate any glitch shape. Symmetric glitches, n_{g_s}, have an input-dependent polarity; where glitch polarity is determined by how the DAC input signal crosses threshold values where glitch transitions occur (i.e. rising or falling) while glitch amplitudes remain symmetric in both directions. For asymmetric glitches, $n_{g_{\bar{s}}}$, both the glitch polarity and amplitude depend on whether the DAC input is falling or rising (i.e. rising glitched transitions may have different polarity and amplitude than falling glitched transitions). A symmetric glitch is modeled as

$$n_{g_s}(w(t)) \triangleq \sum_{i=1}^{N_{T_s}} \left(g_i * \Delta y_i\right)(t)\,, \tag{6}$$

where $*$ denotes convolution, N_{T_s} is the number of transition glitches, g_i is a LTI filter determining the shape of glitch i and

$$\Delta y_i(t) = \frac{1}{\tau}(H(Q(w(t)) - T_i) - H(Q(w(t-\tau_i)) - T_i))$$

with $H(\cdot)$ the Heaviside step-function, T_i a threshold value where a glitch is triggered and $T_i = T_j$ only when $i = j$. A set time-delay $\tau_i > 0$ defines the glitch width and height (here τ_i is chosen such that $\tau = \tau_i = \tau_j$ for all i, j; which means unit-area rectangular pulses). For the more general asymmetric glitch model $n_{g_{\bar{s}}}$, see [13].

As the time-delay $\tau \to 0$, the glitch response converges to the impulse response. This in turn, allows for the net glitch area A_i to be determined solely by the DC-gain of the LTI filters g_i as

$$A_i = \lim_{s\to 0} s\frac{1}{s}\frac{1}{\tau_i}\frac{1 - \mathrm{e}^{-\tau_i s}}{s}\mathcal{L}(g_i)(s) = \mathcal{L}(g_i)(0)\,, \tag{7}$$

where $\mathcal{L}$ denotes the Laplace operator.

The model parameters are fitted to the measured response of a 16-bit Texas Instruments DAC8544 DAC. The number of symmetric glitch transitions for this DAC was set to $N_{T_s} = 2^{16} - 1$, as there is a minor glitch at every least-significant bit (LSB). The DAC also exhibits major, asymmetric glitches at code intervals of 4096, then the number of asymmetric glitched transitions is therefore $N_{T_{\bar{s}}} = 16$.

3) Complete non-linear DAC model: Element mismatch n_{em} is modeled as an additive static non-linearity given by

$$n_{em} = \delta\,\mathrm{INL}(w)\,, \tag{8}$$

where the static non-linear function $\mathrm{INL}(w)$ is called the integral non-linearity [9,12] defined by

$$\mathrm{INL}(w) \triangleq \frac{\tilde{y}(w) - \delta T(w)}{\delta}\,, \tag{9}$$

where $\tilde{y}(w)$ are measured DAC output values corresponding to an input value w obtained to reflect DAC output deviation from the ideal quantisation value (3) due to element mismatch (without accounting for glitches). From (9) we therefore get the following DAC output model

$$\tilde{y}(w) = y(w) + \delta\,\mathrm{INL}(w)\,. \tag{10}$$

To incorporate the effect of glitches into the non-linear DAC model, the dynamic non-linearity n_g is introduced. Let $n_g \triangleq n_{g_s} + n_{g_{\bar{s}}}$ denote the effect of the symmetric and asymmetric glitches [13,24], the DAC output (10) can then be modified by postulating the following DAC output model

$$\tilde{y}(w(t)) = y(w(t)) + n_{em}(w(t)) + n_g(w(t))\,. \tag{11}$$

The model of the non-linear quantiser is shown in Fig. 2.

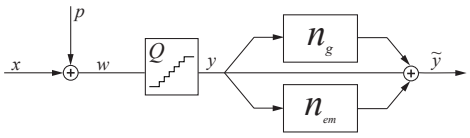

Fig. 2. Non-linear DAC model.

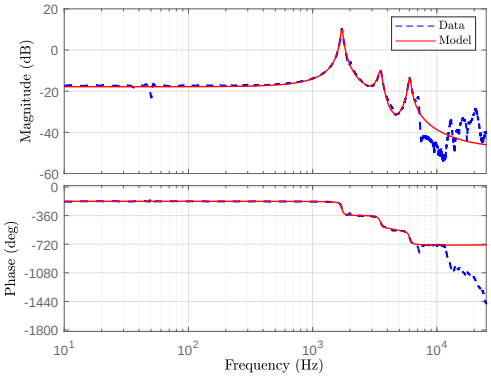

Fig. 3. Nano-positioning stage frequency response.

B. Anti-Aliasing and Reconstruction Filters

The reconstruction and anti-aliasing filters, $W_r(s)$ and $W_a(s)$, are second-order Butterworth filters. They are taken to be identical, $W_r(s) = W_a(s)$. The reconstruction filter reduces repeated spectra due to sampling, and tends to reduce quantisation error. Similarly, the anti-aliasing filter reduces signal content above the Nyquist-frequency before sampling. These filters are usually designed with the objective of sufficiently attenuating frequency content above the Nyquist-frequency. However, here the control scheme in [25] is utilised, where these filters are included in the synthesis of the control law. In the event the cut-off frequency is found to be significantly lower than the Nyquist-frequency these filters not only form a part of the control law, but contribute to attenuating disturbances and averaging the dithered response as well. The filters have a transfer function of the form

$$W_a(s) = W_r(s) = \frac{{\omega_c}^2}{s^2 + \sqrt{2}\omega_c s + {\omega_c}^2} \ , \tag{12}$$

where ω_c is the cut-off frequency, chosen to be a control law synthesis parameter as detailed in Sec. IV-A.

C. Nanopositioning Stage

Common positioning stage designs suffer the presence of lightly damped resonances in their response [21,25]. The dominant dynamics can be represented by a single mass-spring-damper system when operated in piston mode [21]; but here the stage frequency response model, $G_d(s)$, is a seventh-order model fitted to experimentally measured data. It captures lightly-damped resonances corresponding to various vibrational modes of the stage geometry and design [21]. This is shown in Fig. 3, where the lightly-damped resonances occur at 1.7, 3.5, 6.0 kHz, and the model response plateaus at -45 dB for higher frequencies.

D. Additional Instrumentation

1) Amplifier: The piezoelectric actuator driver modeled is a Piezodrive PDL200 voltage amplifier with a gain of 20 V/V. The amplifier has a first-order frequency response

$$W_A(s) = \frac{\omega_A}{s + \omega_A} \ , \tag{13}$$

where the cut-off frequency is equal to $\omega_A = 1/(24C_a)$ and C_a is the load capacitance. Since the actuator has a capacitance of $C_a = 293$ nF, the cut-off frequency is therefore at $\omega_A = 2\pi\, 22.8$ krad/s.

2) Displacement Sensor: The displacement feedback sensor modeled is the SIOS LSV 120NG laser interferometric displacement sensor. It is a homodyne Michelson design counting discrete fractions of the laser wavelength in order to measure displacement; hence it inherently quantises the measurement and is equivalent to an ADC. Laser interferometers are the fundamental measuring technique for length and all dimensional quantities in nanometrology [26]. The sensor has a first-order frequency response as in (13), with a cut-off frequency $\omega_S = 2\pi\, 5$ Mrad/s. The sensor bandwidth is much larger than the sampling rate of the simulation and therefore operates as a gain stage with unity sensitivity for the entire operational system bandwidth (i.e. $W_S \approx 1$ V/m).

III. DITHERING

By a (periodic) dither we understand any bounded, periodic, and sufficiently regular function $p : [0, \infty) \to \mathbb{R}$, e.g. a sinusoidal, square-wave, or saw-tooth signal. In this paper, p is a periodic high-frequency (HF) signal. Now let $n(w)$ denote any function of bounded variation (e.g. $Q(w)$ in (3)), then using a τ-periodic dither signal p we may define the smoothed non-linearity $N(x)$ as

$$N(x) \triangleq \int_{\mathbb{R}} n(x+v)\mathrm{d}F_p(v) \ , \tag{14}$$

where $F_p(v)$ is the amplitude distribution function of p given by $F_p(v) = \frac{1}{\tau}\mu\{t \in [0,\tau) \mid p(t) \leq v\}$ with μ the Lebesgue measure, see [18]–[20] for a detailed mathematical treatment of dither signals. The Lebesgue-Stieltjes integral in (14) is equivalent to the time-average over one period τ of the periodic dither, where x is assumed to be constant for the duration of the period [20]:

$$\int_{\mathbb{R}} n(x+v)\mathrm{d}F_p(v) = \frac{1}{\tau}\int_0^\tau n\left(x + p(t)\right)\mathrm{d}t \ . \tag{15}$$

The error due to the assumption of x being piece-wise constant with duration τ, goes to zero as $\tau \to 0$. Given that F_p is an absolutely continuous distribution, the averaging effect of the dither p on the non-linearity $n(w)$ is generally found by evaluating the Lebesgue-Stieltjes integral of the form:

$$\int_{\mathbb{R}} n(x+v)\mathrm{d}F_p(v) = \int_{\mathbb{R}} n(x+v) f_p(v)\mathrm{d}v \ , \tag{16}$$

where $f_p(v)$ is the amplitude density function, defined as:

$$f_p(v) \triangleq \frac{\mathrm{d}}{\mathrm{d}v} F_p(v) \ . \tag{17}$$

The smoothed non-linearity $N(x)$ can be found as the convolution of the function $n(w)$ and the amplitude density function of the dither. A signal with uniform amplitude density

$$f_p(v) = \frac{1}{2A}\text{rect}\left(\frac{v}{2A}\right) = \begin{cases} \frac{1}{2A} & |v| \leq A \\ 0 & |v| > A \end{cases} , \qquad (18)$$

where A is the periodic dither amplitude, is an example of a signal with an absolutely continuous amplitude distribution function $F_p(v)$. One realisation of such a signal is the triangle-wave, which is the dither used in the simulations. Considerations regarding dither frequency choice include the guarantee for dither-induced disturbances to be filtered out at the system output by the control law. For example, a certain dither frequency choice may excite higher-order resonance modes of the positioning stage. However, this does not exclude the choice validity as long as the control law design is able to attenuate consequent disturbances sufficiently, as detailed in Sec. IV-B. Essentially, if a dither is to be generated through the DAC, the sampling rate should be at least 5-10 times higher than the dither frequency for the discrepancy between the continuous and discrete-time description to be small [27]. If the ratio between the sampling frequency and dither frequency becomes too small, discrete-time effects dominate. Hence, the dither frequency should be chosen as high as possible to minimise the approximation error from the piece-wise assumption on x in (15), but at least 5-10 times below the sampling rate to avoid discrete-time artefacts. Accordingly, the chosen dither frequency at 49 kHz has an adequate margin for hardware operation, similar to the implementation described in [12]. In Sec. V-B, dither amplitude is increased progressively to minimise the peak-to-peak residual error in reference tracking.

IV. CONTROL LAW

A. Synthesis Design

Nanopositioning devices are used for motion control, and the control objective is to track a reference signal. Ideal tracking performance is achieved when

$$y_d = r \;\Rightarrow\; T(s) = 1 \,,$$

where $y_d(s)/r(s) = T(s)$ is the complementary sensitivity function of the system, y_d is the plant displacement, and r is the reference signal, as seen in Fig. 1. Hence, a typical performance criterion for a motion control system is the flatness of $|T(j\omega)|$.

The measurement to be used for trajectory tracking is the displacement of the sample platform. Accordingly, a control scheme for the system should use output feedback. Several output-feedback control schemes exist that can achieve good tracking performance [28]. Here, the damping integral (DI) control scheme [25] is chosen. The scheme is advantageous since it requires only an integrator and an all-pole low-pass filter. The control law parameters are the integral gain and the filter cut-off frequency. As there are already low-pass filters in the control loop due to the need for an anti-aliasing filter W_a and reconstruction filter W_r, these can be used as a part of the control law, and then it is only necessary to implement an integrator in addition.

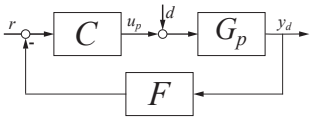

Fig. 4. Control law structure; here u_p is the plant input and d is the plant input disturbance.

Consequently, we consider two cases: In the first case both the low-pass filter and integrator are implemented without regard to the existing anti-aliasing W_a and reconstruction W_r filters. Here, the cut-off frequency for W_a and W_r is set to the nominal design cut-off frequency based on the Nyquist criterion (half the sampling rate) with an added margin to ensure sufficient suppression of repeated spectra due to sampling. In the second case, the filters W_r, W_a are incorporated in the control law synthesis, and there is only a need to implement an integrator in addition. The cut-off frequency for W_r, W_a found when using this configuration is typically much lower than what would nominally be chosen (by the Nyquist criterion). This is beneficial for a system with digital control implementation as the attenuation of aliasing and quantisation error effects from the DAC is improved.

A general control law is specified using the feed-forward filter $C(s)$, the feedback filter $F(s)$, and is applied to the plant $G_p(s)$ as shown in Fig. 4. The complementary sensitivity function is then found to be

$$\frac{y_d}{r}(s) = T(s) = \frac{G_p(s)C(s)}{1 + F(s)G_p(s)C(s)} \,. \qquad (19)$$

The configuration for the nominal case is then

$$C_i(s) = \frac{{\omega_c}^2}{s^2 + \sqrt{2}\omega_c s + {\omega_c}^2} \, \frac{k_i}{s}, \qquad (20)$$

where k_i is the integral gain, ω_c is the cut-off frequency for the filter. The parameters k_i and ω_c are tunable, but the filters $W_r(s) = W_a(s)$ are set to a fixed cut-off frequency at 250 kHz (keeping a margin of 50% the Nyquist-frequency when the sampling rate is 1 MHz).

The configuration in the second case, DI-incorporated, is

$$C_i(s) = \frac{k_i}{s} \,, \qquad (21)$$

where k_i is the integral gain. In the synthesis, $C(s)$ is combined with the filters $W_r(s) = W_a(s)$, and the parameters k_i and ω_c are tunable; therefore, ω_c is now the cut-off frequency for $W_r(s)$ and $W_a(s)$.

The feed-forward filter, feedback filter, and plant are then:

$$\begin{aligned} C(s) &= C_i(s) \,, \\ F(s) &= W_a(s)W_S(s) = W_a \,, \\ G_p(s) &= -W_r(s)W_A(s)G_d(s) \,. \end{aligned}$$

There are two tunable control law parameters $\theta_c = [\omega_c \; k_i]^{\mathrm{T}}$, the filter cut-off frequency ω_c and the integral control law gain k_i. The damping integral control scheme uses the cost-function $J(\theta_c) = \|1 - |T(j\omega; \theta_c)|\|_2$ to achieve the

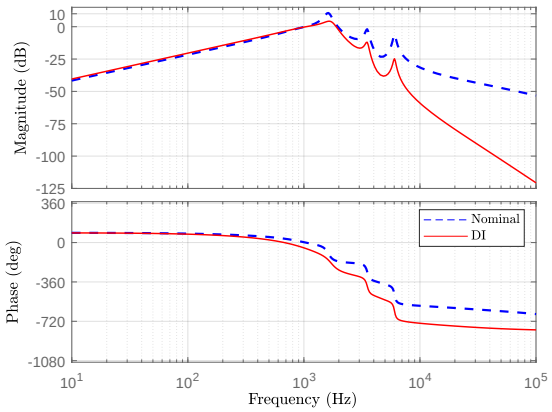

Fig. 5. Transfer function from plant input disturbance d to plant output y_d (nominal vs. DI control law).

flattest response of the complementary sensitivity function. The optimal control law parameters are found by solving $\theta_c{}^* = \arg\min_{\theta_c} J(\theta_c)$ subject to $\mathrm{Re}\{\lambda_i\} \in \mathbb{R}_-$ where $\{\lambda_i\}$ is the set of eigenvalues for the closed-loop system. The solution for the first (nominal) filter configuration (with $C_i(s)$ from (20)) is found to be: $\omega_c = 2\pi\,1230$ rad/s, and $k_i = 7.58 \times 10^3$. Whereas, in the second (DI-incorporated) case where W_r, W_a is incorporated in the control law synthesis (with $C_i(s)$ from (21)), the solution is: $\omega_c = 2\pi\,2050$ rad/s, and $k_i = 6.60 \times 10^3$.

B. Performance Measure

Closed-loop analysis shows that both control synthesis choices are stable with comparable bandwidths lower than the dither frequency. The nominal design has a bandwidth of ($BW_{Nom} = 2\pi\,1740$ rad/s) while the DI-incorporated design has a bandwidth of ($BW_{DI} = 2\pi\,1828$ rad/s). The performance measure adopted in [25] is used to evaluate the disturbance rejection ability of both synthesis designs from Sec. IV-A. The accumulated disturbances due to DAC non-linearities are viewed as an effective disturbance d added to the plant input u_p as in Fig. 4. The effect of d over u_p is investigated by breaking the loop at u_p; the loop transfer function is

$$L(s) = C(s)F(s)G_p(s)\,.$$

This yields the sensitivity $S(s)$ of plant input u_p to a disturbance d:

$$u_p = (1 + L(s))^{-1} d = S(s)d\,.$$

Accordingly, the transfer function $D(s)$ from a disturbance d to the plant displacement y_d is given as:

$$y_d = G_p(s)S(s)d = D(s)d\,. \tag{22}$$

Fig. 5 reflects the enhanced disturbance rejection performance of the DI-incorporated synthesis choice over the nominal one. Both designs show very good attenuation at low frequencies up to the system bandwidth. However, the DI-incorporated design exhibits superior performance attenuating disturbances at dither frequency prior to the plant input u_p.

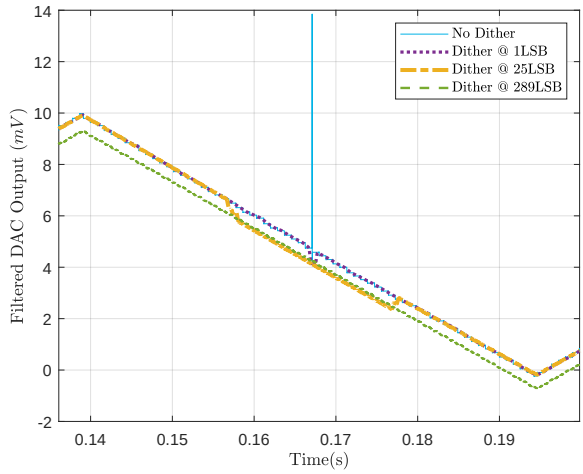

Fig. 6. Glitched DAC response to dither in open-loop: Excerpt showing an averaged (filtered) dithered glitch at various peak-to-peak dither values.

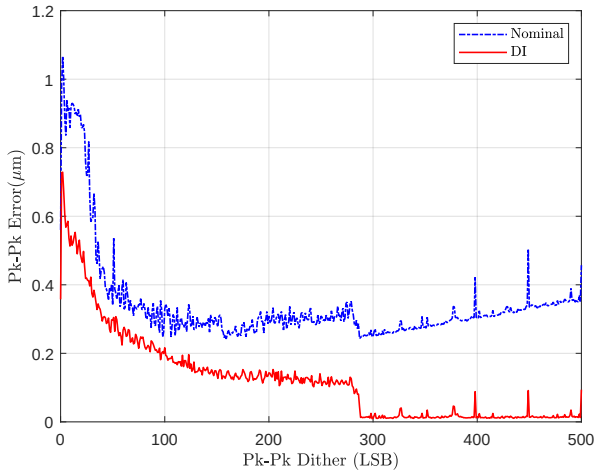

Fig. 7. Glitched disturbance rejection performance in closed-loop: residual error due to DAC non-linearities in response to dither pk-pk variation (nominal vs. DI control law).

V. RESULTS

A. Simulations

The reference signal driving the filtered DAC output in Fig. 6 and being tracked in Figs. 8 and 9, is a 9 Hz triangle-wave with an amplitude of 0.05% of the DAC full range (10 V) and no DC offset. The periodic dither signal was set to be a 49 kHz triangle-wave. Glitch properties are chosen to present an accurate model fitted to the hardware device glitch measurements and sampling rate limitations as addressed in [13]. Therefore, the glitch duration in the model was set to $\tau = 1$ μs (matching a single sample period since the simulation is run at 1 MHz sampling rate). The area for the major (asymmetric) glitches was set to -60.6 nVs for the rising input, and 51.9 nVs for the falling input. The area of the minor (symmetric) glitches was set to ± 2.40 nVs. Where for a given glitch of area A_i, the resultant glitch height is A_i/τ.

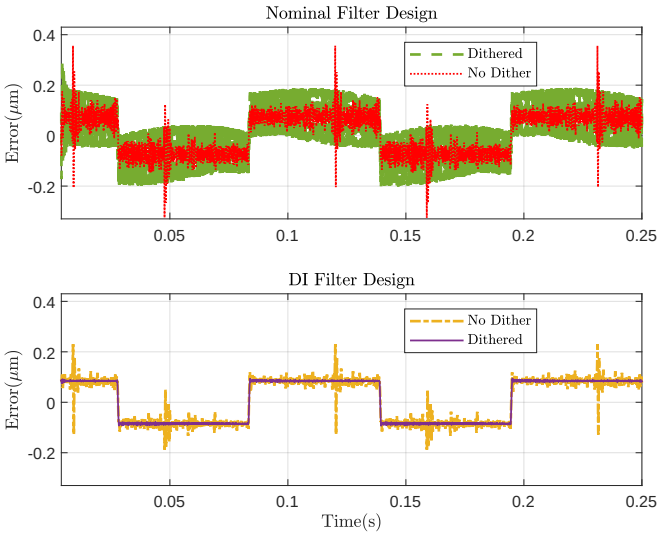

Fig. 8. Low-pass filtering design choice effect on closed-loop tracking performance (nominal vs. DI control law). Dithered at 289 LSB pk-pk

B. Results and Discussion

Fig. 6 captures the essence of the averaging effect due to dithering and filtering. That is to transform a glitch from a large-amplitude disturbance with a short duration (impulse-like), to a smaller amplitude disturbance with a longer duration (step-like).

In general, a control law is bandwidth limited, and will therefore attenuate a step-like disturbance more effectively. In the case of a 289 LSB pk-pk dither shown in Fig. 6, it can be seen that if the dither is sufficiently large, the duration of the step-like response is so long that it appears to be a DC offset at the DAC output when compared to ideal DAC operation. The exact definition of sufficient dither amplitude to achieve complete glitch mitigation is non-linearly dependent on relative values of both the input and glitched transition levels, e.g. the same input with non-zero DC offset may require a different dither amplitude to be mitigated. Hence achieving such sufficiently large dither in closed-loop can be utilised to completely mitigate the disturbance since high-frequency transients can be completely suppressed by the subsequent filtering stage. Evidently, tracking a ramped input using an integral law exhibits an inherent finite time delay and steady-state error between the reference and controlled position [25,27]. Consequently, even with an ideal DAC, the tracking error is expected to have a pulse-train-shaped component. This error is referred to as $e_{benchmark}$, which has no component due to DAC non-linearities. It is therefore crucial to assess the glitch mitigation performance for a non-linear DAC due to dither injection and filtering in isolation of reference tracking error typical of the integral law implemented. To obtain $e_{benchmark}$ and isolate it, the system in Fig. 1 is simulated with the DAC bypassed (i.e. $\tilde{y} = x$). Now, it is possible to determine the residual tracking error component due to DAC non-linearities e_r when operating the system in Fig. 1 with the non-linear DAC operated in the closed-loop as $e_r = e - e_{benchmark}$. Hence, an adequate

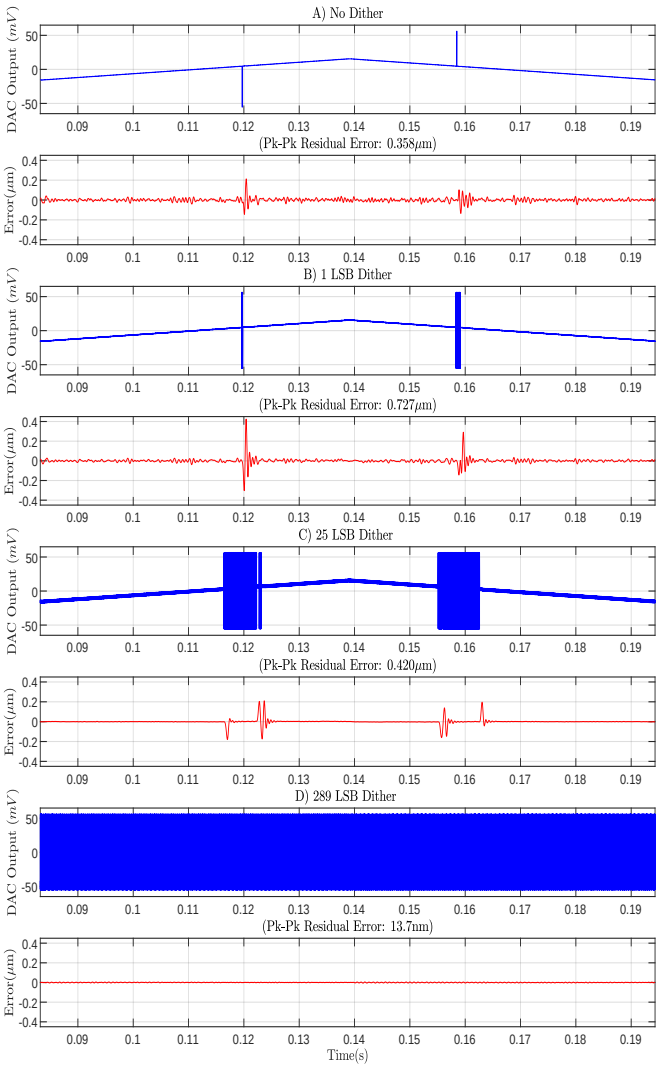

Fig. 9. Illustrative time-traces of residual error progression due to dither amplitude variation.

performance metric to be minimised by sweeping dither amplitude is the peak-to-peak residual error e_r. Accordingly, dither amplitude is increased gradually as simulated in Fig. 7 to determine a sufficiently large dither minimising the peak-to-peak residual error due to DAC non-linearities. The lowest dither amplitude to do so is recorded to be 289 LSB; where the peak-to-peak residual error is 3.83% its value at 0 LSB (i.e. no dither) for the DI-incorporated case. Such reduction entails that $e_r \approx 0$, indicating almost complete glitch mitigation. In addition to the significance of dither amplitude choice, complementary attention should be given to the low-pass filtering action. Since filtering works in tandem with dither injection to achieve adequate averaging and disposal of the unwanted high-frequency dither content at the output stage. To showcase the significance of low-pass filtering design choice as raised in Sec. IV, Fig. 8 illustrates a time trace of the overall tracking error e depicting the superior performance of the DI-incorporated filter design approach to the nominal one as Fig. 7 confirms. Even though

the glitch has been averaged for both designs and stability is guaranteed. The enhanced ability of the DI-incorporated design to suppress high-frequency dithered-induced disturbance content prior to the nano-positioning actuation stage, reduces the overall error $e(t)$ as indicated in Fig. 5. The dithered DI-incorporated approach exhibits a typical response of a DI control law with the glitch completely rejected. Fig. 9, illustrates dither role in glitch rejection when operated in closed-loop. Note the fundamental effect of introducing dither even at 1 LSB as seen at the DAC output $\tilde{y}$; it invokes glitches with both polarities to occur at each glitched transition level (as opposed to no dither, Fig. 9-A). This is due to the fact that the input trend (rising/falling) is alternated by the injected dither. The worse performance in Fig. 9-B (as compared to Fig. 9-A) is due to the controller speed to reach steady-state. Larger dither amplitudes cause wider sectors of the input to excite major glitches (i.e. reason for transformation into longer-duration step-like disturbances after filtering). This is in correspondence with the filtered DAC output operated in open-loop from Fig. 6. Moreover, larger dither amplitudes cause multiple minor glitches to occur at the dither frequency (i.e. ramped portion of the DAC output becomes thicker) and, therefore to be filtered out at the output. Hence, smaller tracking error is achieved even when no major glitches are excited. Fig. 6 explains the opposing polarity of the transients in the error signal across the edges of said sectors apparent the most in Fig. 9-C. Tracing the error evolution across time, the first transient is an attempt to compensate for an "upward" stepped disturbance. The tracking settles back as it reaches steady-state, then tries to compensate for a "downward" stepped disturbance at the second transient, and so on. Furthermore, it is observed that complete dither rejection is achieved when the dither modulates the occurrence of glitches at a frequency well-attenuated by complementary filtering. Fig. 9-D, depicts a DAC performance comparable to ideal operation with complete glitch mitigation.

VI. CONCLUSIONS

A method for glitch mitigation for a non-linear DAC used in closed-loop applications was demonstrated. The glitches pose a resolution limit in precision digital control systems. A simulation model of a closed-loop nano-positioning system with a non-linear DAC was presented. The simulation results demonstrated significant mitigation of the glitches; achieved by utilising large-amplitude high-frequency dither and low-pass filtering. The dithering and averaging of the glitch responses effectively converted the short-duration, large-amplitude impulse-like behaviour to a long-duration, small-amplitude step-like disturbance, which made it possible to attenuate the disturbance using an integral control law. This translated to a smaller tracking error and hence better overall performance.

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