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Abstract

The goal of this project is to gain competence in low-power power supply design by building a functioning prototype that balances various requirements while maintaining a reasonable cost. The project involves detailed hardware design, simulation, prototype production, and testing.

A theoretical review and comparison of suitable converter topologies are performed, and the Flyback converter design is explained. The hardware design section covers the selection of components, their functions in the circuit, and the printed circuit board (PCB) layout considerations.

The design is produced and built. The troubleshooting process is laid out, and several tests are performed and discussed to evaluate the prototype.

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Chapter 1

Introduction

1.1 Background and Motivation

Easee ASA is focused on designing and constructing a low-power, dual-output, isolated power supply for their next-generation charging robot. The decision to develop a custom power supply unit (PSU) in-house is driven by the desire to build strategic in-house competence, achieve long-term cost savings, and ensure the production of high-performance, high-quality and compliant end products.

1.2 Objectives

The goal is to obtain competence in low-power power supply design by building a functioning prototype that balances various requirements while maintaining a reasonable cost. The project involves detailed hardware design, simulation, prototype production, and functional testing, including performance data, thermal performance, waveforms, output ripple measurements, and EMI and ESD tests.

1.3 Organization

This work is organized in the following chapters:

- **Chapter 2.** Provides a brief overview of low power isolated AC/DC power supply units most common topologies.
- **Chapter 3.** Goes into the implemented Flyback circuit in detail and provides a basis for the design choices.
- **Chapter 4.** Shows the hardware product of this work and contains the results from all the performed tests under different parameter variations.
- **Chapter 5.** Evaluates the obtained results, identifies strong points and the shortcomings, and provides suggestions for improvements and further development.

Chapter 2

Theory

This chapter outlines the theoretical framework for addressing the problem at hand, detailing various considerations and potential solutions. It categorizes different topologies of low power isolated DC/DC power supply units, discusses their advantages and disadvantages, and sets the stage for the design phase. This chapter is written with the help of ***perplexity.ai***.

2.1 Low power isolated DC/DC power supply overview

Low power isolated DC/DC power supply units are designed to provide galvanic isolation between the input and output sides, while delivering relatively low output power levels, typically under 100W.

2.1.1 Common topologies

The most common topologies used for low power isolated supplies are:

- Flyback converter: This is one of the simplest isolated topologies, using a transformer with a single winding for energy transfer. It is well-suited for multiple output voltages and is cost-effective for power levels around 50-100W [13].
- Forward converter: Similar to the Flyback, but with a separate output inductor instead of using the transformer's leakage inductance. More efficient than Flyback at higher power levels [3].
- Push-pull: These use two switching transistors driving the primary winding in a push-pull fashion. Suitable for medium power levels up to a few hundred watts [16].

2.1.2 Features

- Provide galvanic isolation using a transformer, ensuring safety from high input voltages [4].
- Multiple output voltages are common, with dual outputs being a frequent requirement [21].
- Output power levels typically range from a few watts to around 50-100W [3].
- High efficiency is achieved through synchronous rectification and advanced control ICs [14].
- Compact size due to high switching frequencies (100kHz - 1MHz) [4].

2.1.3 Applications

- Powering analog and digital circuitry that requires isolation from high voltages [4].
- Gate drivers for power semiconductor devices like IGBTs and MOSFETs [14].
- Instrumentation and control systems requiring multiple isolated supply rails [21].

- Medical devices requiring patient isolation for safety [19].

While more complex isolated topologies like LLC resonant converters are used for higher power levels above 200W, the Flyback, forward, and push-pull converters offer simple and cost-effective solutions for low power isolated applications.

2.2 Advantages and disadvantages of different topologies

We take a deeper look at the previously mentioned topologies in order to choose a suitable solution for the problem at hand.

2.2.1 Isolated Flyback converter

An isolated Flyback converter is a type of switched-mode power supply (SMPS) topology that uses a transformer to provide galvanic isolation between the input and output. This isolation ensures that there is no direct electrical connection between the input and output, which is crucial for safety and noise reduction in many applications. The Flyback converter operates by storing energy in the transformer's magnetic field during the switch-on period and releasing it to the output during the switch-off period. This makes it functionally similar to a buck-boost converter but with the added benefit of isolation.

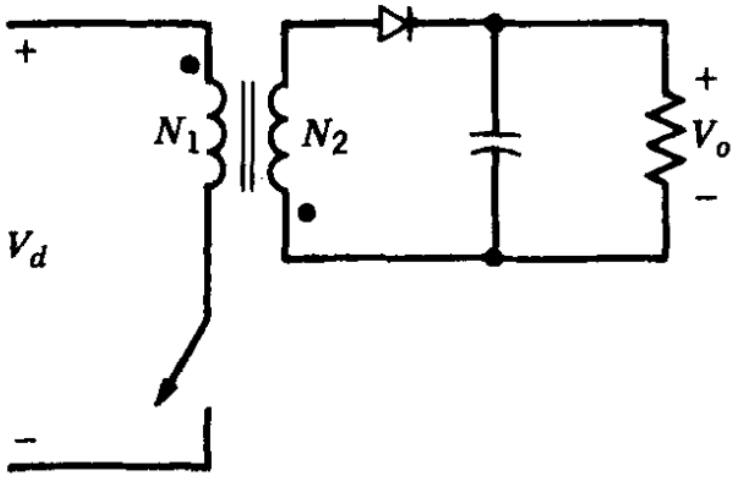


Figure 2.2.1: Topology of Flyback converter [14].

2.2.1.1 Advantages

1. Simplicity and Low Component Count: The Flyback converter has a simple circuit design with a minimal number of components, making it cost-effective for low power applications [11].

2. Multiple Isolated Outputs: The topology allows for easy generation of multiple isolated output voltages with little additional circuitry, which is beneficial for applications requiring multiple power rails [14].

3. Wide Input Voltage Range: Flyback converters can accommodate a wide input voltage range, making them suitable for both step-up and step-down operations [20].

4. Isolation and Safety: The transformer provides galvanic isolation between the input and output sides, ensuring safety from high input voltages and preventing ground loops [4].

2.2.1.2 Disadvantages

1. Efficiency Limitations: Flyback converters use the core less efficiently, leading to larger core size, weight, and cost, especially as power levels increase. Their efficiency is generally lower than non-isolated converters due to the presence of transformers and optocouplers [5]. Therefore, Flyback converters are typically used for low power applications below 150W. Beyond this power level, other topologies like forward converters are more efficient and practical [3].
2. Component Stress: The Flyback converter experiences higher peak currents and voltage stresses on the switching elements and output capacitors, which can lead to higher component costs and reduced efficiency [20].
3. Output Ripple and Noise: They tend to have higher output ripple and noise, which may require additional filtering to meet stringent noise requirements in sensitive applications [3].
4. Regulation and Performance: The regulation and transient performance of Flyback converters are generally inferior to non-isolated converters due to the presence of transformers and optocouplers, which add complexity and potential points of failure [5].

While Flyback converters offer simplicity and cost-effectiveness for low power isolated applications, their efficiency, component stress, and performance limitations make other topologies more suitable for higher power levels above 150W.

2.2.2 Isolated Forward converter

An isolated forward converter is a type of switched-mode power supply (SMPS) converter that uses a transformer to provide galvanic isolation between the input and output, allowing for voltage step-up or step-down based on the transformer's turns ratio. This converter transfers energy directly from the primary to the secondary side of the transformer during the switch's

conduction phase, unlike the Flyback converter which stores energy in the transformer core and releases it during the "off" period.

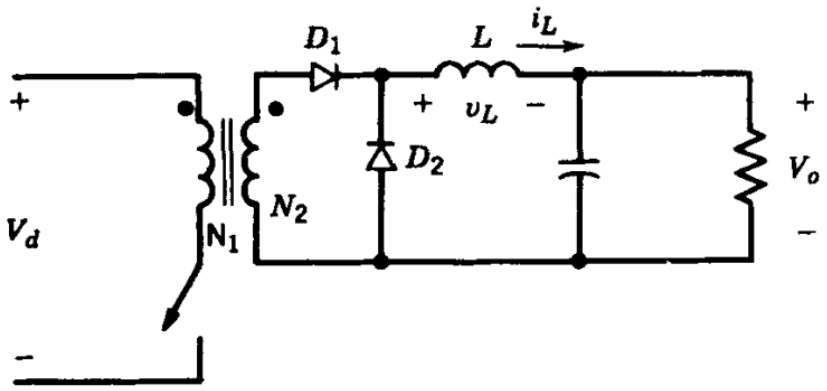


Figure 2.2.2: Topology of idealized forward converter [14].

2.2.2.1 Advantages

1. Reduced Output Ripple: The output inductor and freewheeling diode in forward converters help maintain a fairly constant output current, significantly reducing secondary ripple current and output voltage ripple [10].
2. Higher Efficiency: Forward converters generally exhibit higher efficiency compared to Flyback converters, especially at higher power levels. This is due to lower core losses and reduced leakage inductance losses [3].
3. Reduced radiated EMI: Forward converters do not require an air gap in the transformer core, reducing radiated EMI [18].

2.2.2.2 Disadvantages

1. Increased Complexity and Cost: Forward converters require additional components such as an output inductor and freewheeling diode, making them more complex and expensive to build compared to Flyback converters [3].

2. Minimum Load Requirements: Forward converters may require a minimum load to maintain regulation, especially in applications with multiple outputs. Operation in Discontinuous Conduction Mode (DCM) can lead to increased losses and stress on the switch and transformer [12].

3. Transformer Design: The transformer design in forward converters is critical and more challenging, as it must handle the continuous transfer of energy without saturating. This might require additional components such as reset winding or active clamp circuits to prevent transformer saturation [3].

Isolated forward converters are a robust choice for applications requiring efficiency, isolation and low output ripple. However, their increased complexity, cost, and specific component requirements must be considered during the design phase to mitigate their inherent limitations.

2.2.3 Isolated Push-pull converter

An isolated push-pull converter is a type of switched-mode power supply (SMPS) converter that uses a transformer to provide galvanic isolation between the input and output. This converter topology is characterized by its use of a center-tapped transformer and two transistors that alternately switch on and off, creating a push-pull effect. This design allows for efficient power transfer and voltage conversion, making it suitable for applications requiring isolation and high efficiency.

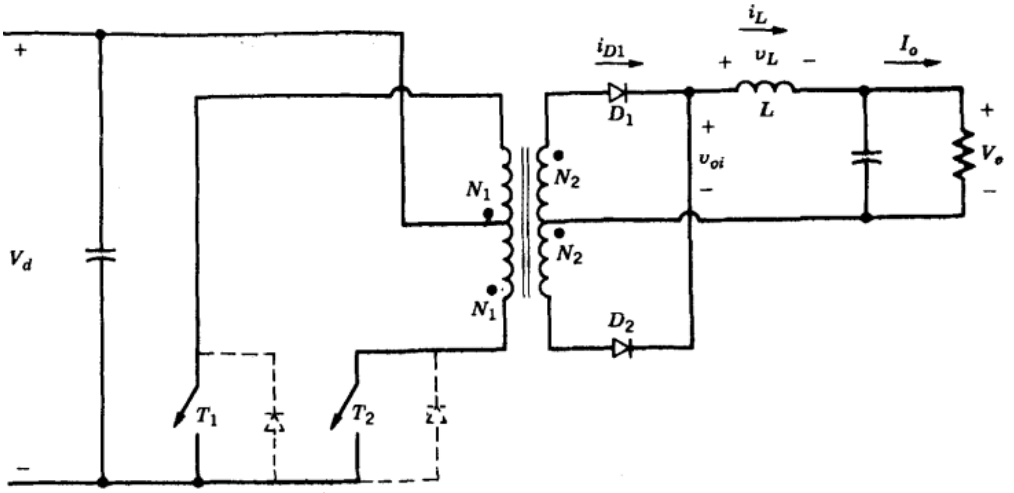


Figure 2.2.3: Topology of Push-pull converter [14].

2.2.3.1 Advantages

1. High Efficiency: Push-pull converters are known for their high efficiency, especially in high-power applications. The transformer in a push-pull converter operates in a bipolar magnetization mode, which reduces leakage inductance and copper resistance loss, leading to higher efficiency [15].

2. Good Voltage Utilization: Push-pull converters have excellent voltage utilization, maintaining high output power even at low input voltages. This makes them suitable for applications with low input voltage requirements, such as DC/AC inverters and DC/DC converters [15].

3. Stable Output Characteristics: The output voltage waveform of a push-pull converter is very symmetrical, providing good voltage output characteristics. This results in a high transient response speed and low output voltage ripple [15].

4. Low EMI Emissions: The balanced configuration of push-pull converters helps in reducing electromagnetic interference (EMI) emissions, making them suitable for applications

with strict EMI regulations[15].

2.2.3.2 Disadvantages

1. High Voltage Stress: The two switching devices in a push-pull converter must withstand high voltage stress, often more than twice the operating voltage. This requirement limits their use in high-voltage applications [6].
2. Core Saturation Risk: If the two forward converters in a push-pull topology are not completely symmetrical, a DC bias can occur, leading to core saturation. This can cause large excitation currents and potentially damage the switching devices [9].
3. Complex Transformer Design: The transformer in a push-pull converter requires a center-tapped primary winding, which can be more complex and costly to design and manufacture compared to other topologies [9].

Push-pull converters are a versatile and efficient, offering significant advantages such as high efficiency and good voltage utilization. They are particularly beneficial in applications requiring galvanic isolation and low EMI emissions. However, their design complexity, high voltage stress on switches and potential for core saturation necessitate careful engineering. Despite these challenges, push-pull converters remain a popular choice in various high-power and isolated power supply applications due to their robust performance and reliability.

2.3 Power supply specifications and considerations

The power supply for the next-generation charging robot are not finalized at the time of writing this thesis. Nonetheless, the preliminary specifications are sufficient to design and construct a prototype to acquire competence and familiarity with power supply concepts and challenges.

The requirements for the power supply are summarized in the following table:

Output	Voltage [V]	Current [A]	Isolation	Reference
1	14.5	1.2	Yes	PE
2	14.5	0.5	No	N

Table 2.3.1: Power supply preliminary specifications.

In addition, the power supply needs to operate between -30°C to +85°C ambient, AC input between 85-265 VAC and comply with EMC standards in EN 61000-6-1, EN 61000-6-3 and EN 50470-1.
In light of these requirements and the previous paragraphs in this chapter, the Flyback converter is likely the best topology to use. The reasons for this statements is summarized as follows:

- Power Level and Cost-Effectiveness. The power supply requirements are relatively low, with output power levels at 14.5V with 1.2A and 0.5A, around 24.65W. The lower efficiency of the Flyback topology is tolerable at this power level as the total amount of heat generated due to losses, can be easily managed. Eliminating the need for more efficient topologies that can be more complex and expensive.
- Multiple Output Voltages. Flyback converters can easily supply multiple isolated output voltages with minimal additional circuitry, which is needed according to the requirements. The other topologies mentioned in this chapter can also achieve this but would require more complex circuitry.
- Galvanic Isolation. Flyback converters inherently provide galvanic isolation through the use of a transformer, ensuring that there is no direct electrical connection between the input and output. This isolation is required on one of the outputs of the power supply (14.5V, 1.2A, PE). The other topologies also satisfies this requirement.

- Simplicity and Low Component Count. The simplicity of the Flyback converter's design, with a minimal number of components, makes it easier to design, build, and maintain. The Straightforward design of the transformer reduces the possibility of transformer related issues. This simplicity translates to lower costs and higher reliability, which is important for the development and prototyping phase of the power supply for the charging robot. This will also allow for easier troubleshooting and serve as a good stepping stone to build competence in power supply design.

2.4 Flyback topology in-depth

This section provides an in-depth exploration of the Flyback circuit design, including a simulation of idealized circuit. The majority of this section relies on ***RECOM AC/DC Book of Knowledge*** [17].

The Flyback converter converts an input voltage into a regulated output voltage by storing energy in the transformer core gap during the ON time and transferring it to the secondary during the OFF time. Technically the transformer consists of two coupled inductors as the energy transfer is not by true transformer action. This is shown in figure 2.4.1.

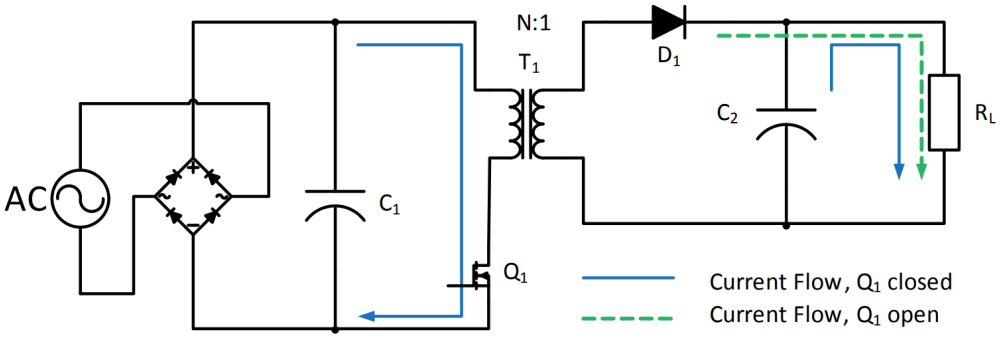


Figure 2.4.1: Isolated Flyback Converter Simplified Schematic [17].

For a power supply without PFC, the rectified mains input voltage will be between 126VDC and 320VDC, but the output voltage is typically between 3.3V and 24V.
The big advantage of a Flyback transformer design is that the turns ratio decides the fundamental input/output voltage ratio as shown in equation 2.1. The variable mark-space PWM controller on the input power stage can then easily compensate for any variation in input voltage or output load. Duty cycles higher than 0.5 are possible with the Flyback topology, but in general should be avoided to reduce the average current in the output diode.

$$V_{\text{out}} = V_{\text{in}} \left(\frac{1}{N} \frac{\delta}{1-\delta} \right), \text{ valid for } V_{\text{in}} < \text{ or } > V_{\text{out}} \tag{2.1}$$

So for a universal input AC/DC with a minimum input range of 90VAC (no PFC, so 126VDC when rectified) and an output voltage of 14.5VDC, the transformer turns ratio would be chosen to be 8:1. At this input voltage, the PWM would have 50% duty cycle. At the highest input voltage of 265VAC (370VDC when rectified), the PWM would have a 25% duty cycle. The relevant relationships are shown in equation 2.2.

$$\text{Duty Cycle} = \frac{V_{OR}}{V_{OR} + V_{IN}} \tag{2.2}$$

Where the reflected output voltage, V_{OR}, equals (V_{out} + $V_{Drop,D1}$) multiplied by the turns ratio, N. Given the above values, V_{OR} = (14.5V + 1V) x 8 = 124V.
Finally the large inductive spike on the primary winding when S1 is turned off places a lot of strain on the switch as shown in equation 2.3. In addition, there is a resonant oscillation caused by the interaction between the leakage inductance of the transformer, the primary winding capacitance and the body-diode capacitance of the switching FET. As all of these values are very small, the resonant frequency is very high – typically in the region of tens of MHz. This not only causes serious EMC problems but can induce very high currents to flow.

$$V_{pk} = V_{in,DC} + \frac{V_{out} + V_F}{N} + I_{pri}\sqrt{\frac{L_{lk}}{C_{pri} + C_{oss}}} \tag{2.3}$$

Where V_F is the forward voltage drop across the secondary diode, N is the turns ratio, I_{pri} is the primary current, L_{lk} is the total leakage inductance, C_{pri} is the primary winding capacitance and C_{oss} is the FET drain-source capacitance as shown in figure 2.4.2.

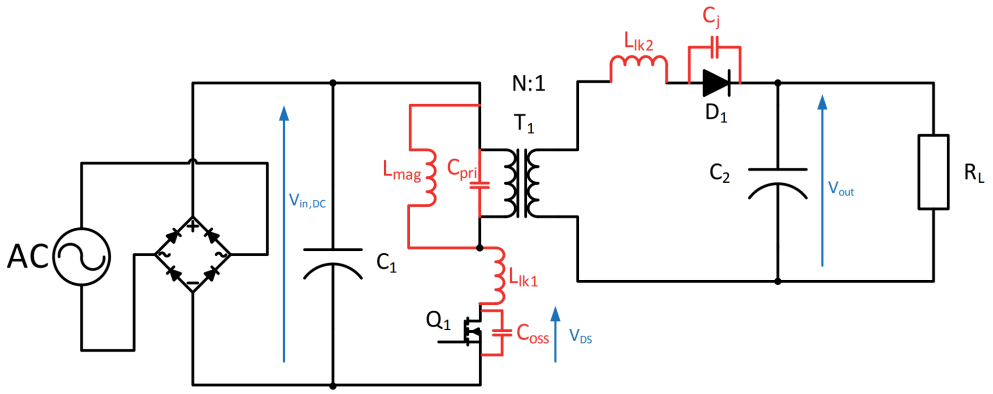


Figure 2.4.2: Single ended Flyback showing parasitic elements (in red) [17].

The effect of these parasitic elements means that the switching voltage and current waveforms will not be clean as shown in figure 2.4.3.

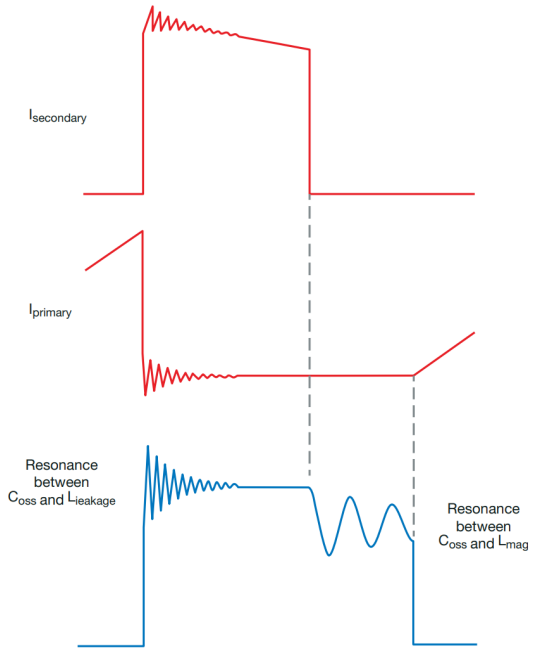


Figure 2.4.3: Voltage and current resonances as a result of the parasitic elements [17].

2.4.1 Snubber Networks

2.4.1.1 High side Snubber

To absorb this damaging high frequency parasitic oscillation, a snubber is often required. The most common arrangement on the high side is a RCD (Resistor-Capacitor-Diode) snubber as shown in figure 2.4.4.

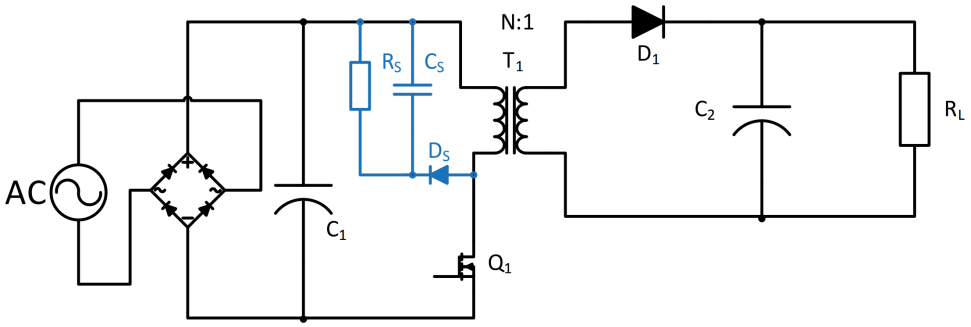


Figure 2.4.4: RCD snubber circuit (shown in blue) [17].

The capacitor and resistor absorb the energy of the resonance ringing and cause it to decay more rapidly. The recovery diode is typically a standard power diode (not a fast diode) as a relatively slow reverse recovery time (Trr) also helps to dampen out the ringing. The negative current that flows during this recovery time allows the snubber capacitor to dampen the ringing more effectively by absorbing current on the positive cycle and delivering current on the negative cycle despite the diode rectification. The power dissipated in the snubber network is highest at minimum Vin and full load as shown in equation 2.4

$$P_{\text{diss,snubber}} = \frac{1}{2} f L_k I_{\text{peak}}^2 \frac{V_{\text{CS}}}{V_{\text{CS}} - n(V_{\text{out}} + V_D)} \tag{2.4}$$

Where f is the switching frequency and V_{CS} is the voltage across the snubber capacitor Cs. The optimum value of the snubber capacitance found with equation 2.5 is also dependent on the snubber resistor, Rs found with equation 2.6, as they both operate together to absorb the

ringing energy.

$$C_s[\mu F] = \frac{V_{CS}}{\Delta V_{CS} f R_s} \tag{2.5}$$

Where ΔVCs is the ripple voltage across the snubber capacitor (typically chosen to be 5%-10% of VCs).

$$R_s = \frac{V_{CS}^2}{\frac{1}{2} f L_k I_{peak}^2 \frac{V_{CS}}{V_{CS} - n(V_{out} + V_D)}} \tag{2.6}$$

If needed, a resistor in series with the diode can be added to damp the resonant peak between the primary leakage inductance and the snubber capacitor. This is called a R2CD snubber network.

2.4.1.2 Ringing Snubbers

Besides reducing the voltage stress on the main switching transistor, snubbers can also be used to damp ringing in the primary FET as shown in figure 2.4.5 or secondary rectifier diode as shown in figure 2.4.6.

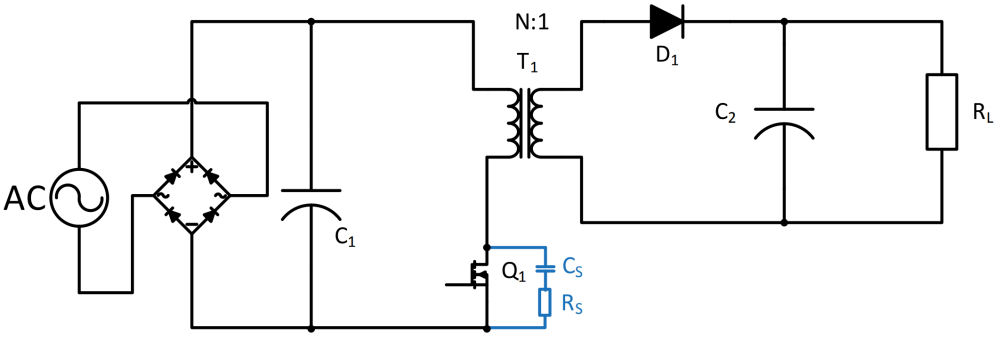


Figure 2.4.5: Primary snubber (low side snubber) [17].

The low side snubber provides damping for the LC resonance of the switching FET caused by the interaction of the primary leakage inductance and the MOSFET junction capacitance when the FET is turned off. One way to calculate the required snubber components is to measure the transformer primary inductance with the outputs short circuited using an

inductance meter (or a frequency response analyser) and use an oscilloscope to measure the ringing frequency fr (hold the probe close to, but not touching the drain pin – the probe will pick up the signal without dampening it with the probe's own capacitance) The snubber resistor is calculated with equation 2.7:

$$R_s = 2\pi f_r L_{\text{pri}} \tag{2.7}$$

And the snubber capacitor is calculated with equation 2.8:

$$C_s = \frac{1}{2\pi f_r R_s} \tag{2.8}$$

The power dissipation in the snubber resistor is calculated with equation 2.9:

$$P_{\text{diss,Rs}} = f C_S V_{DS}^2 \tag{2.9}$$

Where f is the switching frequency (not the ringing frequency) and V_{DS} is the peak FET voltage.

Ringing also occurs on the secondary output diode when it becomes reverse biased, so it can be useful to also put a snubber across it as shown in figure 2.4.6:

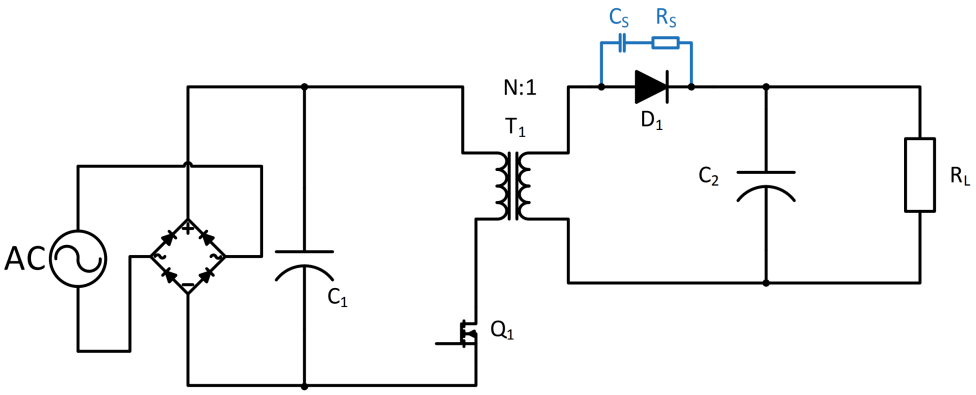


Figure 2.4.6: Output diode snubber (shown in blue) [17].

The peak ringing voltage across the secondary side diode if a snubber was not fitted would

be as in equation 2.10:

$$\text{Diode Peak Voltage Stress, } V_{\text{pk,diode}} = V_{in,\text{max,rectified}} \cdot n + I_{\text{sec}}\sqrt{\frac{L_k 2}{C_j}} \tag{2.10}$$

Where n is secondary to primary turns ratio, Lk2 is the secondary leakage inductance and Cj is the junction capacitance of the diode.

The output capacitor will absorb most of the ringing voltage if it has a low ESR and the PCB track inductance is not too high, but the diode must be able to survive this peak reverse voltage.

Adding the secondary side snubber not only dissipates the energy safely and protects the diode, but reduces the EMI generated by the secondary ringing which can be in the order of 10s of MHz. On the other hand, as the ringing frequency is much higher than the switching frequency, it is relatively easy to filter out without incurring a high power dissipation loss.

Typical values for secondary snubber components are 4x the junction capacitance for the capacitor and a resistor value equal to the term.

2.4.2 Quasi-Resonant Flyback Converter

A Quasi-Resonant (QR) converter can be made to work with most AC/DC topologies, but it is most commonly used as a single ended Flyback. The main difference is that the QR converter PWM timing is dependent on the switch current minima rather than on the output voltage alone as shown in figure 2.4.7. A standard Flyback controller has a fixed PWM frequency which defines when the next cycle starts, but the QR uses a free-running oscillator with variable off time.

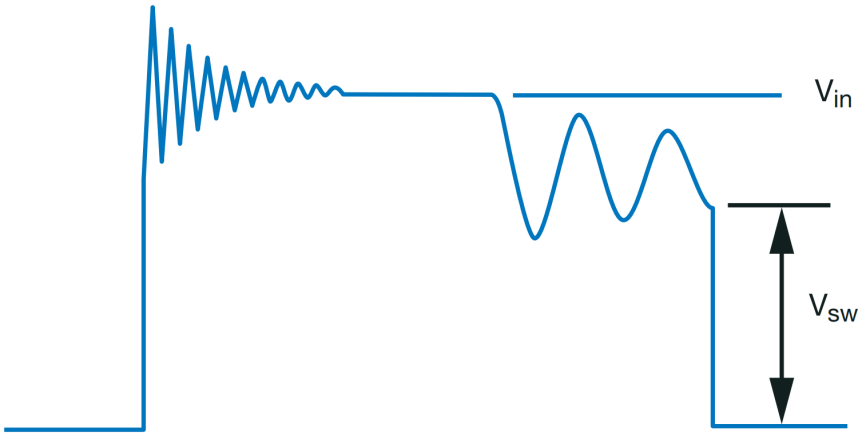


Figure 2.4.7: QR valley switching [17].

As in the standard Flyback topology, the QR topology PWM controller turns on the switch ON to store energy in the transformer core and then turns the switch OFF to allow the energy to be transferred to the secondary. Once the current in the output rectifier diode has fallen to zero, then both input and output winding currents will fall to zero. Any remaining energy in the core will be reflected back into the primary which will start to resonate at a frequency (calculated with equation 2.11) dependent on the primary inductance, L_p , and the lumped drain capacitance, C_D, consisting of the sum of the switch capacitance, the coupling capacitance between the winding and any other stray capacitances.

$$f_{\text{resonance}} = \frac{1}{2\pi\sqrt{L_p C_D}} \tag{2.11}$$

With a primary inductance of 1.475mH and a C_D value of 1.7nF, the resonant frequency will be around 100.5 kHz. The voltage across the (open) switch will be the supply voltage superimposed with this resonant oscillation. By choosing to reset the PWM cycle when this voltage is at minimum (valley switching) means that the effective voltage across the switch will be below the supply voltage. This means that the switch now has a much lower turn-on voltage stress and lower turn-on current, both of which will give a measurable increase in efficiency.

Another advantage of QR operation is that the PWM period timing changes slightly with each cycle depending on the accuracy of the valley detection circuit. This timing jitter flattens out the EMI spectrum and reduces the peak EMI levels. A reduction of 10dB in the conducted interference levels can readily be achieved compared to a conventional Flyback circuit. A disadvantage of QR operation is that the PWM frequency is load-dependent and frequency limiting or valley-lockout circuits are needed to cope with no-load conditions.

Chapter 3

Hardware Design

This chapter provides an in-depth exploration of the Flyback circuit implementation, including a simulation of idealized circuit. It explains the rationale behind the specific choices made during the design process. The chapter systematically divides the circuit into functional blocks and shows the values of the various components. Furthermore, it illustrates the printed circuit board (PCB) layout and the reasoning behind, it also describes the production process. The majority of this chapter relies on ***Power Integrations (PI) reference design*** [2].

3.1 LTspice simulation

This simulation shown in 3.1.1 builds on the standard Flyback topology and expands it into dual output configuration. It also uses synchronous rectification on one of the outputs while using a simple diode on the other output. It employs a simple PI feedback control and uses a switching frequency of 100 kHz. The components used in the simulation are ideal and the transformer is modeled with four coupled inductors with a coupling factor of 1. The values of the components are based on the specifications of the power supply and on calculations done at a later stage in this chapter.

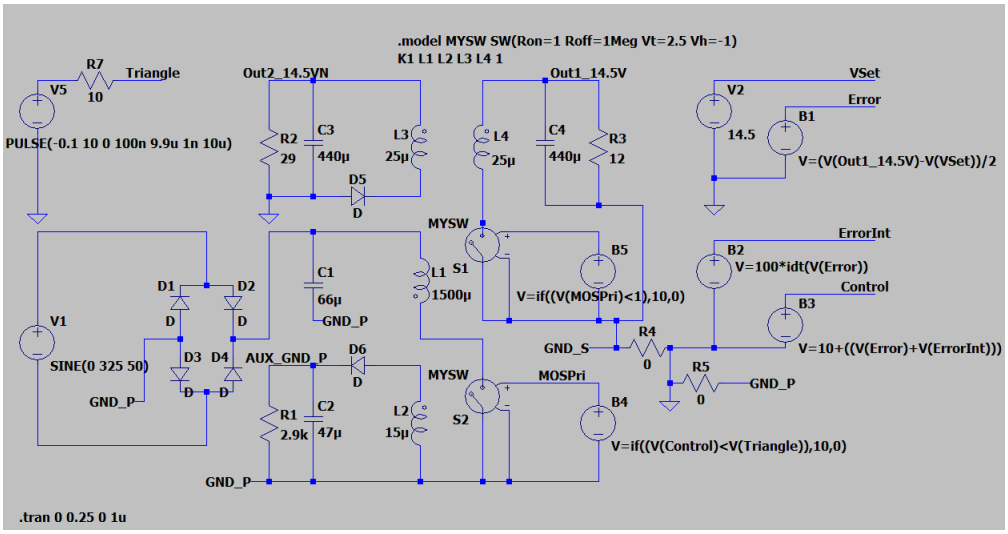


Figure 3.1.1: LTspice simulation

The outputs waveforms shown in 3.1.2 are as expected for output 1 at 14.56V and auxiliary output at 12.2V. While output 2 is at 15.87V (should also be around 14.5V), this indicates that there might be regulation issues without feedback from the second output.

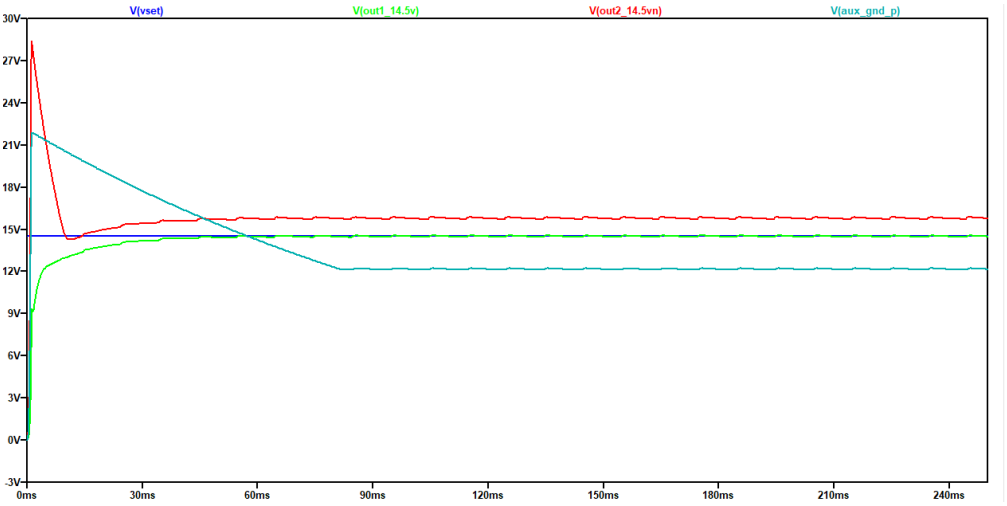


Figure 3.1.2: LTspice simulation outputs

3.2 Flyback circuit design

There is a lot of ways to implement the Flyback topology in regards to control, with/without power factor correction (PFC), with/without active clamp and the level of integration of various parts of the design.
After careful consideration of the available solutions on the market, Power Integrations power management integrated circuits (PMIC) was chosen to base the design on. In particular, InnoSwitch3-EP family. The reasoning behind this choice can be summarized as follows [8]:

- This PMIC family has the same footprint and pin-out with different level of power and breakdown voltages. They are largely interchangeable, which makes the solution flexible and easily modifiable without the need for many changes in the original design.
- This PMIC family combines primary and secondary controllers and safety-rated feedback into a single IC. This high level of integration reduces the component count thus simplifying the design process and manufacturing, but it comes with the drawback of lack of control of the specific implementation of drivers, safety and feedback circuits.
- This PMIC family incorporate multiple protection features including line over and under-voltage protection, output overvoltage and over-current limiting, and over-temperature shutdown. Trying to implement such features without using an off the shelf solution would have expanded the scope of the design process to unmanageable proportions given the time-frame.
- The architecture incorporates a inductive coupling feedback scheme (FluxLink) to transmit output voltage and current information from the secondary controller to the primary controller. This eliminate the need for optocoupler circuitry, reducing the component count even further.
- The primary controller on InnoSwitch3-EP is a Quasi-Resonant (QR) Flyback controller that has the ability to operate in continuous conduction mode (CCM), boundary mode

(CrM) and discontinuous conduction mode (DCM). As mentioned in 2.4.2, using Quasi-Resonant control results in better efficiency and flattens out the EMI spectrum and reduces the peak EMI level.

Figure 3.2.1 and 3.2.2 shows primary and secondary controller block diagram respectively.

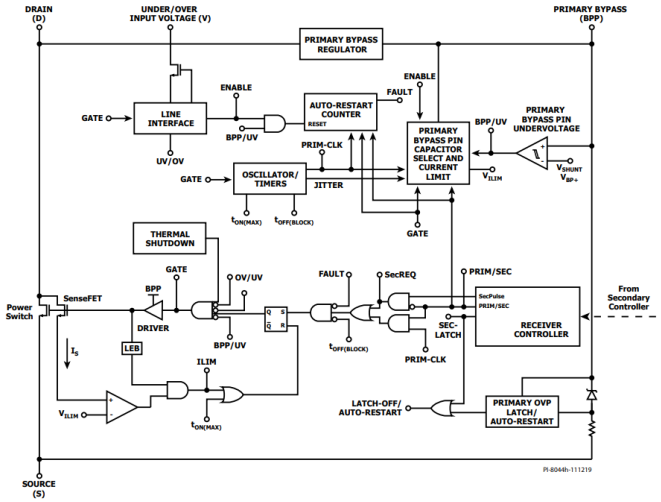


Figure 3.2.1: Primary Controller Block Diagram [8].

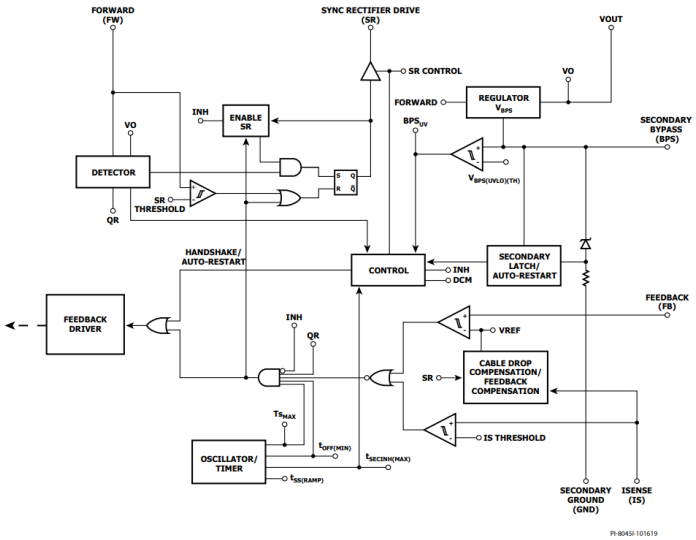


Figure 3.2.2: Secondary Controller Block Diagram [8].

Power Integrations offers PI Expert power supply design software. The software does all the needed calculations and simulations based on the requirements, gives the suggested values for the components and estimates the resulting voltages, currents and temperatures. This software was used for the design, the resulting document is included in A, some adjustments to the components choice based on the desired outcomes (better reliability, larger margins and experimental purposes). This design is implemented in ***Altium Designer*** (electronic design automation (EDA)) software, the design output documents are included in B. INN3675C-H602 is the specific variant chosen from InnoSwitch3-EP family to be used, as it has 25W power capacity and the desired protection features. The target switching frequency is chosen according to PI recommendation found at page 19 of the datasheet. At 65kHz, better thermal performance and a good margin for peak power is achieved [8].

Figure 3.2.3 shows the overall design of the converter and how the different parts interact with each other. In the next sections, each part will be discussed in detail. Figure 3.2.4 shows the schematics of the converter, divided into the functional blocks. Better resolution figure is found B.1.

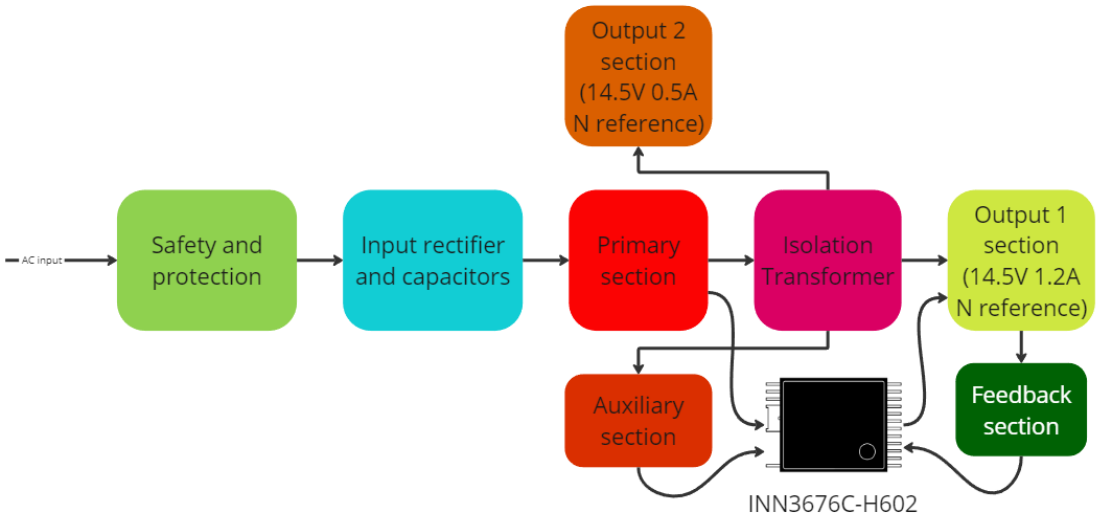


Figure 3.2.3: Converter Block Diagram.

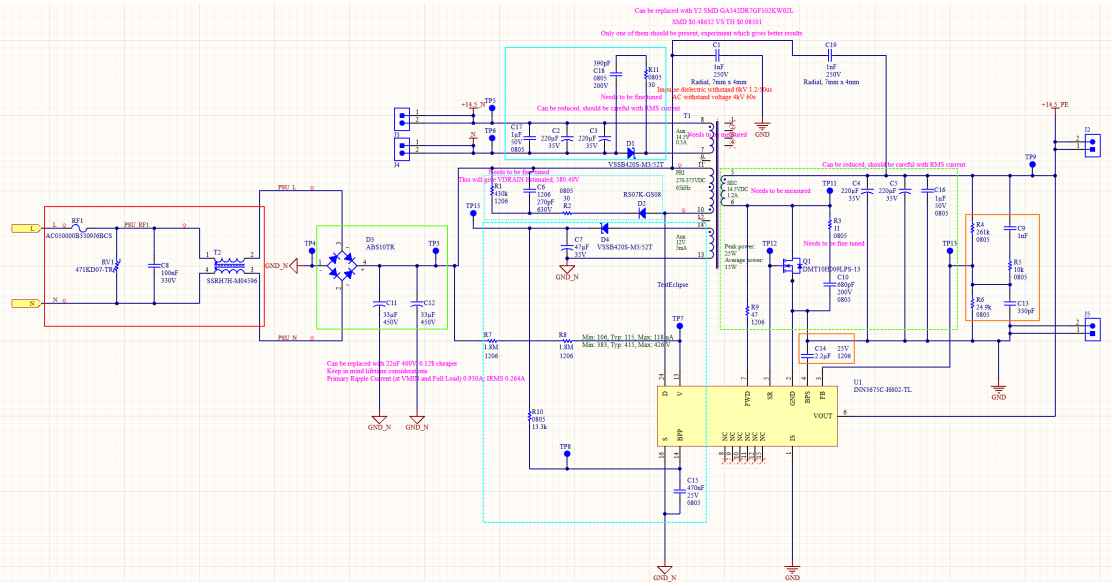


Figure 3.2.4: Converter schematics: Safety and protection(continuous red rectangle), Input rectifier and capacitors (Input rectifier and capacitors), Primary section (dotted blue rectangle), Auxiliary section (dashed blue rectangle), Output 1 section (dashed green rectangle), Output 2 section (solid blue rectangle), Feedback section (continuous orange rectangles).

3.2.1 Safety and protection

Figure 3.2.5 shows the area of the schematics related to safety and protection.

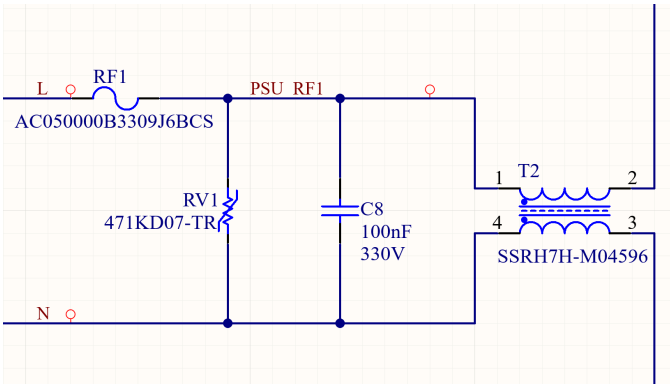


Figure 3.2.5: Safety and protection.

The fusible resistor RF1 has a higher value and power rating than the one suggested by PI Expert (33Ohm vs. 10Ohm; 5W vs. 2W).
The Metal Oxide Varistor RV1 also has a higher energy rating than the one suggested by PI Expert (29J vs. 23J).
The EMI filter components also have higher ratings. The X capacitor C8 has the values of 100nF and 330V vs. 47nF and 250V suggested by PI Expert.
The Common Mode Choke T2 has the value of 59.6mH vs. 6mH suggested by PI Expert.
The Y capacitor C1/C19 has the value of 1nF vs. 0.1nF suggested by PI Expert. The choice between using C1 or C19 (C1 is connected to the secondary side ground while C19 is connected to the secondary winding positive terminal) is a matter of experiment. Which is better is layout dependent and conducted emission chart should be evaluated.
The beefier values for these component are chosen to make sure that we pass the various tests. But this comes with the downside of higher costs and in the case of the fusible resistor more power loss and less optimal manufacturing prosess. There is definitely optimizations to be made here.

3.2.2 Input rectifier and capacitors

Figure 3.2.6 shows the area of the schematics related to input rectifier and capacitors.

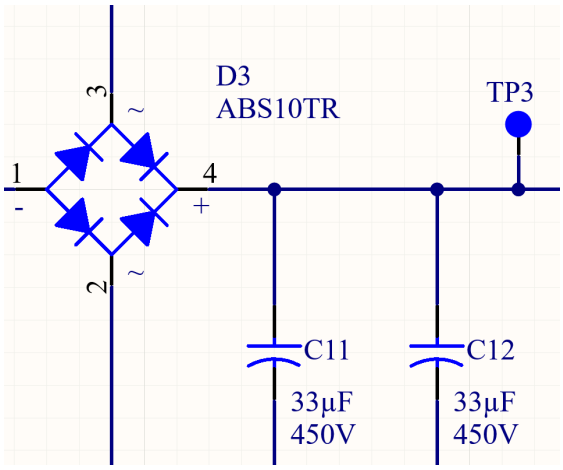


Figure 3.2.6: Input rectifier and capacitors.

The bridge rectifier D3 converts the AC line voltage into the DC voltage seen across capacitors C11 and C12. The chosen bridge rectifier has slightly higher ratings than the one one suggested by PI Expert. The chosen capacitors are larger in value than the one suggested by PI Expert. This is done to increase longevity and performance with downside being cost and size. There is different ways to optimize these components depending on the goals.

3.2.3 Primary section

Figure 3.2.7 shows the area of the schematics related to primary section.

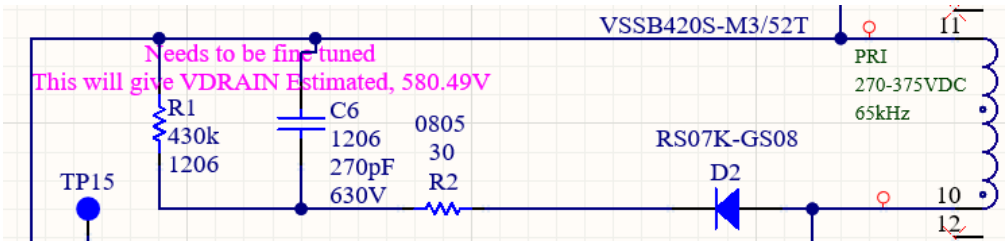


Figure 3.2.7: Primary section.

The transformer T1 pin 11 is connected to the rectified DC bus and pin 10 is connected to the drain of the integrated 725V power MOSFET inside the InnoSwitch3 U1.

An RCD clamp formed by D2, R2, R1 and C6 limits the peak drain voltage to an estimated 646.12V combating the effects of the transformer leakage and trace inductances. This estimated voltage is ca. 11% lower than the breakdown voltage of the MOSFET, which is acceptable.

The values for these components are chosen according to PI Expert suggestions and can be optimized for better performance if this proves necessary after experimental measurements.

3.2.4 Auxiliary section

Figure 3.2.8 shows the area of the schematics related to auxiliary section.

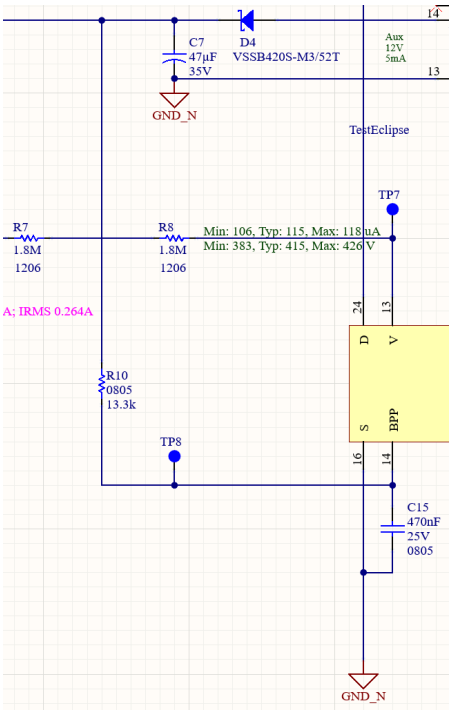


Figure 3.2.8: Auxiliary section.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor C15, when AC is first applied. During normal operation the primary-side block is powered from an auxiliary winding of the transformer T1. The output of the bias winding is rectified and filtered using diode D4 and capacitor C7. Resistor R10 limits current into BPP capacitor from the bias winding.

D4 is upgraded to high voltage Schottky diode for the better recovery characteristics.

C7 is larger in value than the one suggested by PI Expert, following the same reasoning provided in the primary section.

Resistors R7 and R8 provide line voltage sensing and provide a current to U1, which is proportional to the DC voltage across capacitor C3. At approximately 90 VDC, the current through these resistors exceeds the line undervoltage threshold, which results in enabling of U1. At approximately 415 VAC, the current through these resistors exceeds the line overvoltage threshold, which results in disabling of U1.

The values for C15, R7, R8 and R10 are chosen according to PI Expert suggestions. R10 has a different value depending on the PMIC used even within the same family, although not critical and the same value would likely work for different ICs.

3.2.5 Output 1 section

Figure 3.2.9 shows the area of the schematics related to output 1 section.

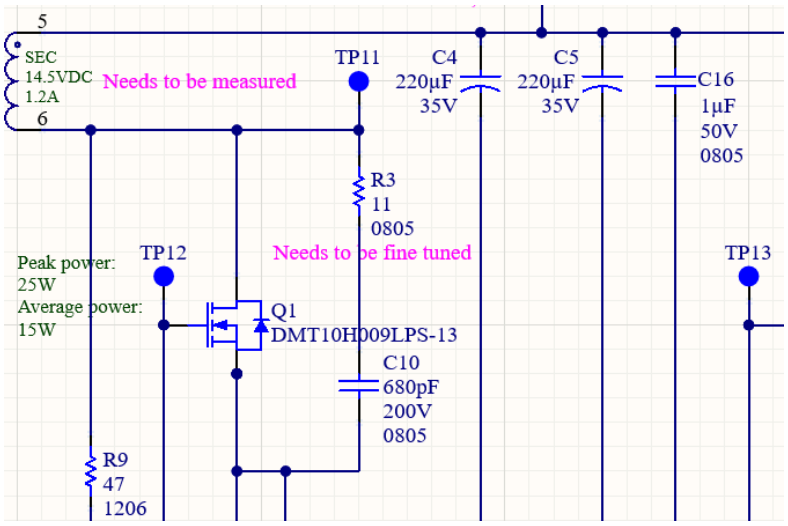


Figure 3.2.9: Output 1 section.

Output rectification for the 14.5V output is provided by synchronous rectification MOSFET Q1. A simple RC snubber network formed by R3 and C10 damps high frequency ringing across the SR FET, which results from leakage inductance of the transformer windings and the trace inductances.

Q1 has better specifications than the one suggested by PI Expert to provide better thermal performance and good margin for peak power.

The gate of Q1 is turned on based on the winding voltage sensed via R9 and the FWD pin of the IC.

The values for R3, R9 and C10 are chosen according to PI Expert suggestions and R3 and C10 can be optimized for better performance if needed.

The output is filtered using capacitor C4 and C5. Again the values of the capacitors are larger than the ones PI Expert suggests, following the same reasoning provided in the primary section.

Capacitor C16 reduces radiated EMI noise.

3.2.6 Output 2 section

Figure 3.2.10 shows the area of the schematics related to output 2 section.

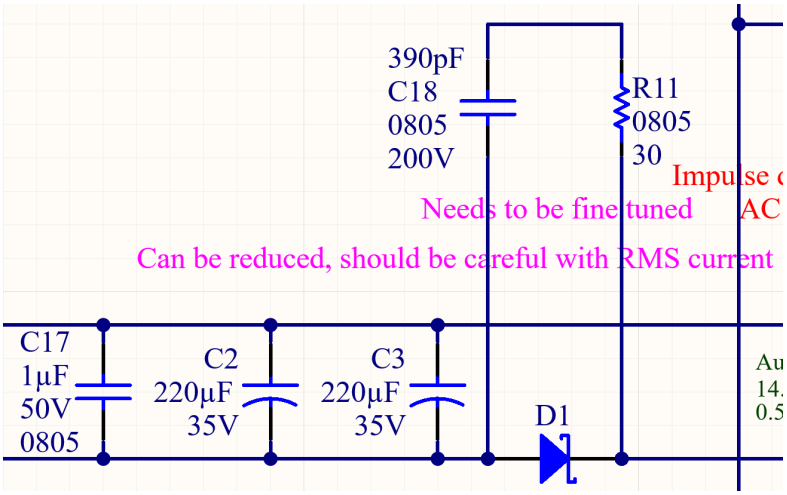


Figure 3.2.10: Output 2 section.

Output rectification for the 14.5V non-isolated output is provided by D1. A simple RC snubber network formed by R11 and C18 damps high frequency ringing across the D1 diode, which results from leakage inductance of the transformer winding and the trace inductances.

D1 is upgraded to high voltage Schottky diode for the better recovery characteristics.

The values for R11 and C18 are chosen according to PI Expert suggestions and can be optimized for better performance if needed.

The output is filtered using capacitor C2 and C3. Again the values of the capacitors are larger than the ones PI Expert suggests. Following the same reasoning provided in the primary section.

Capacitor C17 reduces radiated EMI noise.

3.2.7 Feedback section

Figure 3.2.11 shows the area of the schematics related to feedback section.

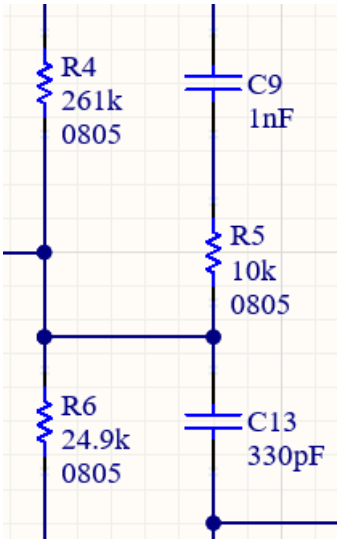


Figure 3.2.11: Feedback section.

Feed forward RC networks comprising capacitor C9 and resistor R5 reduce the output ripple voltage.

Resistors R4 and R6 form a voltage divider network that senses the output voltage. INN3675C IC has an internal reference of 1.266 V.

Capacitor C12 provides decoupling from high frequency noise affecting power supply operation.

The secondary side of the IC is self-powered from the output voltage fed into the VOUT pin and charges the decoupling capacitor C14 via an internal regulator.

The values for R4, R5, R6, C9, C12 and C14 are chosen according to PI Expert suggestions.

Current regulation is not required, thus IS pin is tied to the GND pin.

3.2.8 Transformer specification

The transformer is designed with the help of PI Expert software. The design document mentioned earlier A.5 was revised to change the pin-out of the transformer in order to satisfy clearance requirements. All the other parameters are still the same.

One aspect worth mentioning is the physical placement of the winding relative to the switching elements. We want to put "quiet" turns apart from each other on the primary and secondary side, illustrated in figure 3.2.12. This configuration is aimed at reducing noise coupling, minimizing electromagnetic interference, and enhancing safety and performance of the transformer.

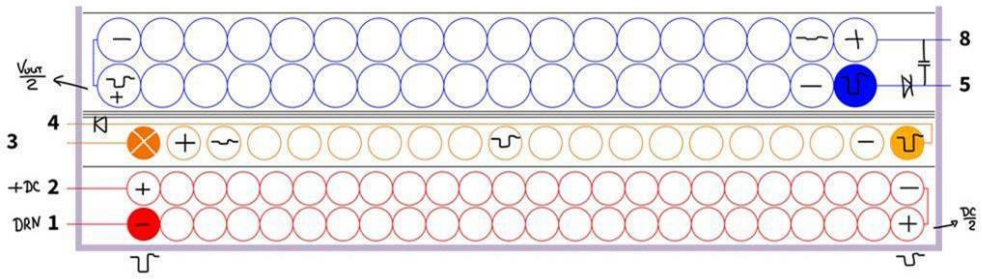


Figure 3.2.12: Transformer winding placement.

3.2.9 Other remarks

- Banana-plug connectors are used on the outputs to make it easier to connect to testing equipment.
- In hindsight, the design should have included an easy way to measure current in different parts of the circuit.
- Test points are added to the design in order to make the troubleshooting process and direct measurements easier.

3.3 PCB Layout

After finishing the design schematics, the next step is component placement on the printed circuit board (PCB). This is also done using ***Altium Designer***. Most of the 2D and 3D models of the components used were already available in the used component library, a few need to be created from the data-sheets as Altium Designer allows modifying the elements or creating new symbols and packages. A four layer board stack-up is used, as it simplifies component placement and routing. Figure 3.3.1 shows a composite of PCB layers, for better resolution B.3 and a view for each layer separately (Layer 1, Layer 2, Layer 3 and Layer 4) can be found here B.4, B.5, B.6 and B.7, respectively.

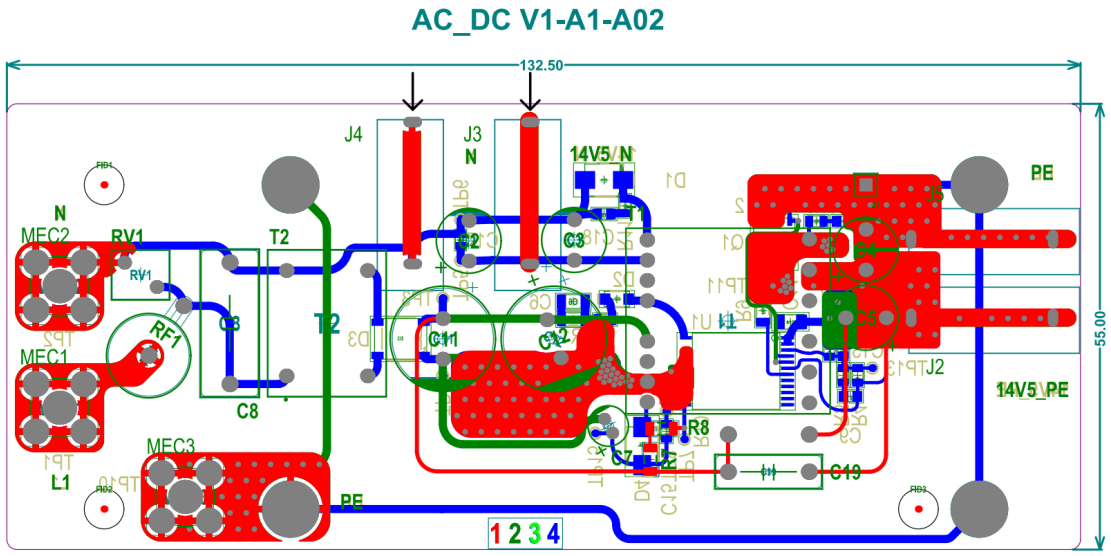


Figure 3.3.1: Composite of PCB layers.

The following PCB layout recommendations [8] page 16-17 and figure 19, were adhered to:

- Maximize source area for good heat sinking. To reduce EMI, minimize the loop from the clamp components to the transformer and IC. keep drain components away from primary bypass (BPP) and under/over input voltage (V) pins circuitry.

- Place under/over input voltage (V) pin sense resistor close to the IC.
- Keep primary bypass (BPP) and secondary bypass (BPS) capacitors near the IC.
- Y capacitor connection to the plus bulk rail on the primary-side for surge protection.
- Keep feedback pin decoupling capacitor close to the IC.
- Place forward and feedback sense resistors near the IC.
- Keep output secondary FET and output filter capacitor loop short.
- Maximize drain area of secondary FET for good heat sinking.
- Use a single-point ground connection from the input filter capacitor to the area of copper connected to the SOURCE pins.

Other general design guidelines are followed, such as:

- As small as possible PCB and shortest tracks possible to reduce cost, minimize parasitic elements and reduce noise susceptibility.
- Mounting through-hole components on the top layer while mounting surface-mount device (SMD) on the bottom layer. In order to make the soldering process easier. Placing test points also on the bottom layer guaranties easy access without being blocked by big through-hole components.
- Rules related to clearance according to The IPC 2221. Rules related to manufacturing and assembly capabilities such as: the minimum distance between the ICs pins, the minimum distance between the tracks, etc.

3.4 Mounting components

The PCB and transformer were externally produced, while the components will be mounted manually. As the PMIC is the major component in the design, most the voltages and currents are generated by it. It also relies on all the external components to be present in order for it to function correctly. This means that the whole PCB should be completely populated before any meaningful test can be performed. The only part that can be tested individually is the transformer; this is done in the beginning of the next chapter.

The through-hole components were mounted first followed by SMDs. All the used components were easy to mount manually and the mounting process went smoothly without any problems. Figures 3.4.1 and 3.4.2 show the fully assembled PCB.

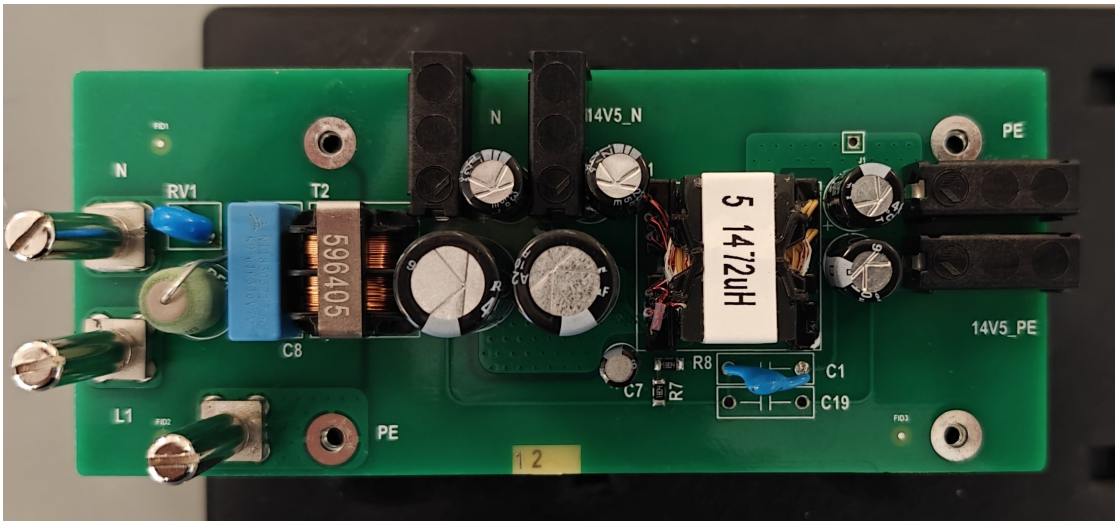


Figure 3.4.1: Fully assembled PCB, top view.

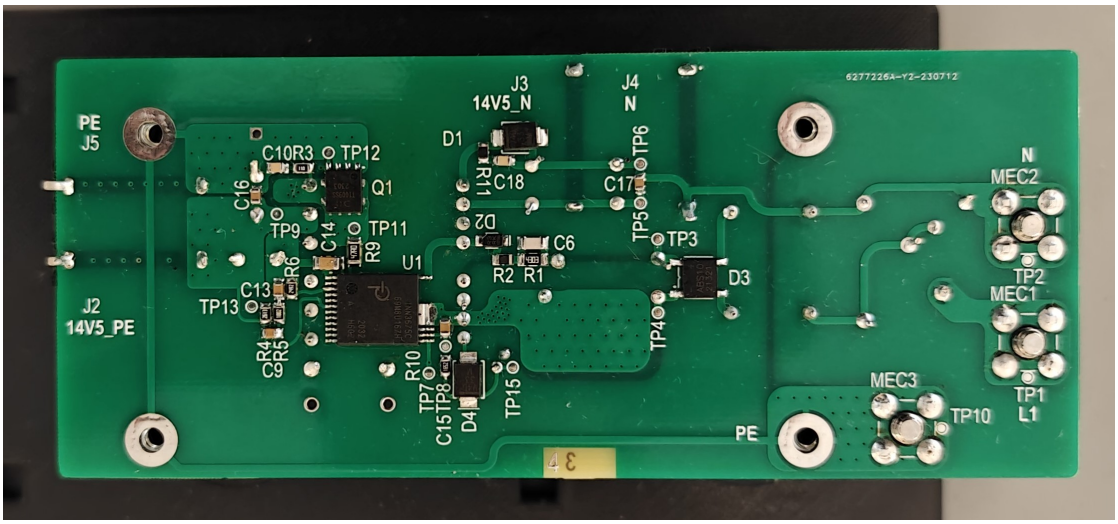


Figure 3.4.2: Fully assembled PCB, bottom view.

Chapter 4

Results and Discussion

This chapter summarizes the obtained hardware results, describes the performed tests, reports the results from them, and discusses their adherence to the expectations.

4.1 Transformer testing

Verifying the basic functionality of the transformer, measuring leakage inductance and parasitic capacitance is a worthwhile test to perform. Obtaining the expected results from these tests, minimizes the likelihood of the transformer acting as a fault source in subsequent tests.

4.1.1 Turns ratio testing

The first test is performed with an oscilloscope, using its signal generator function. A 6V sine wave with the frequency at target switching frequency of 65 kHz is applied on the transformer

primary winding. The corresponding signals of the other winding are measured. Figure 4.1.1 shows the test setup and figure 4.1.2 shows obtained waveforms.

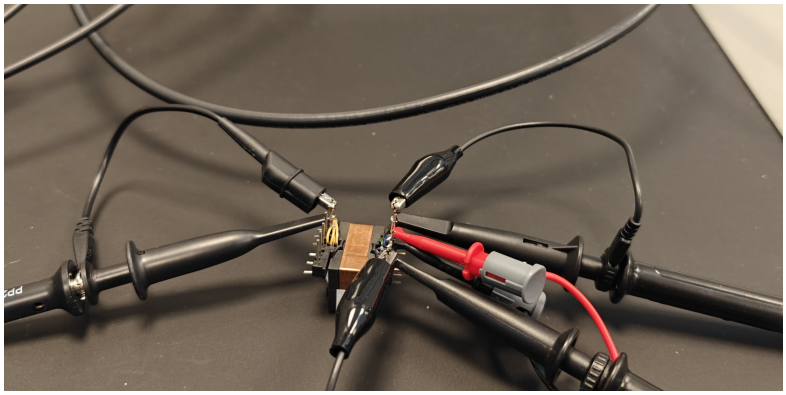


Figure 4.1.1: Turns ratio test setup.

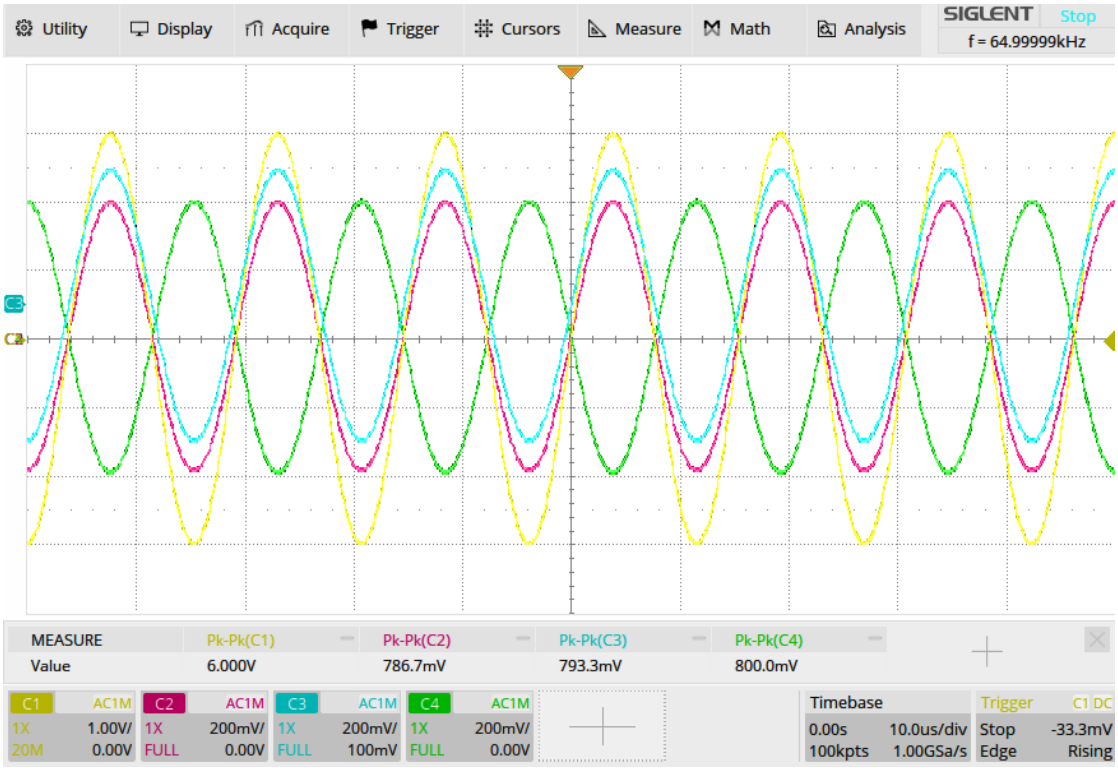


Figure 4.1.2: Turns ratio test obtained waveforms, C1: Signal generator/Primary winding, C2: Output1 winding, C3: Bias winding and C4: Output2 winding.

The obtained waveforms show that Primary winding to Output1 winding has the ratio 7.63 very close to the expected 76:10, Primary winding to Bias winding has the ratio 7.56 also very close to the expected 76:10 and Primary winding to Output2 winding has the ratio 7.5 somewhat close to the expected 76:11. The slight variation can be explained by less than ideal coupling between Primary and Output2 winding, this is not expected to be an issue.

4.1.2 Parasitics measurements

Primary inductance and leakage inductance on the primary side are measured using an LCR meter with frequency at target switching frequency of 65 kHz. The measurements procedure is described here [1] on page 5-6. Figure 4.1.3 shows leakage inductance test setup, all the other winding were open for primary inductance measurement, all the other winding were shorted for leakage inductance measurement.

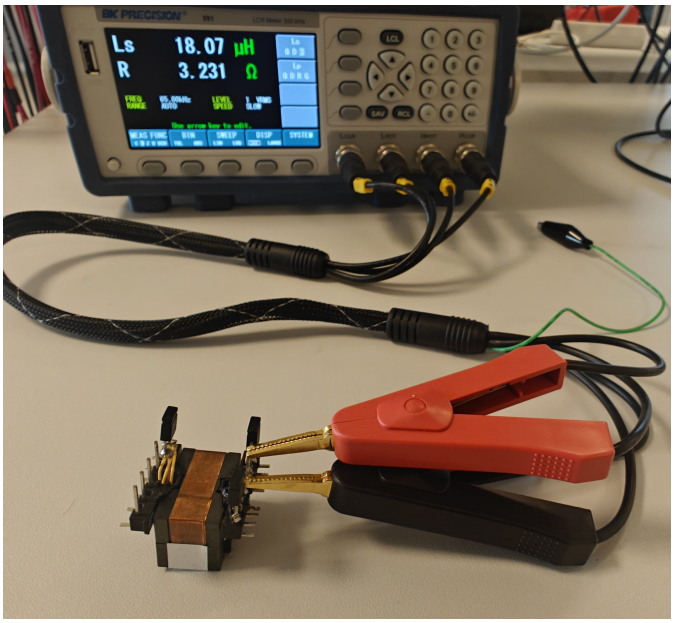


Figure 4.1.3: Leakage inductance test setup (Leakage inductance measurement shown here).

Primary inductance is 1472 uH is close to the expected value 1448 uH, leakage inductance is

18.07 uH is also close to the expected value 16.24 uH. Expected values are found in A.5 on page 12.

Figure 4.1.4 shows parasitic capacitance test setup. Parasitic capacitance between each winding pair measured using an LCR meter and had the following values:

Winding	Primary	Output1	Output2	Bias
Primary	-	47	69	80
Output1	-	-	44	45
Output2	-	-	-	45

Table 4.1.1: Parasitic capacitances in [pF].

These values are small and should not be an issue on their own.

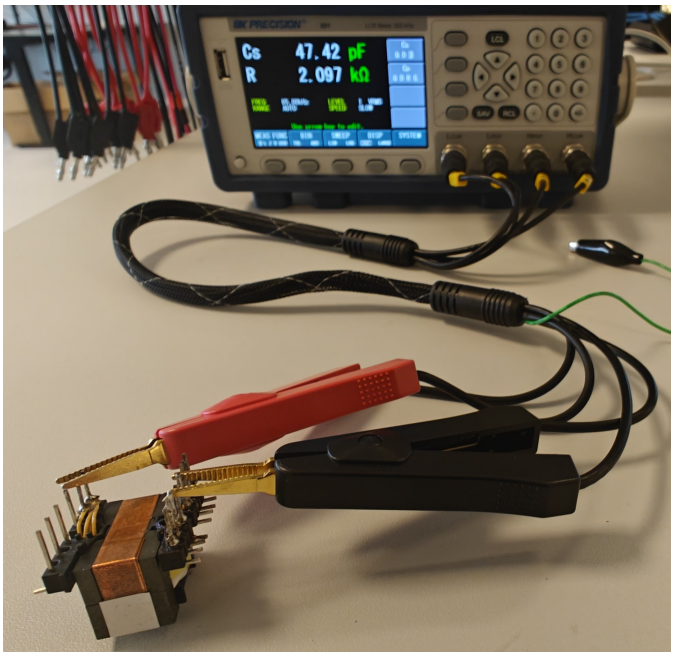


Figure 4.1.4: Parasitic capacitance test setup (Primary winding to Output1 winding shown here).

4.1.3 Circuit testing

The test setup consisted of an isolation transformer, variable voltage source, 3D printed mounting base, a DC load and an oscilloscope. Figure 4.1.5 shows test setup. All the tests were done at an ambient temperature of around 21 C.

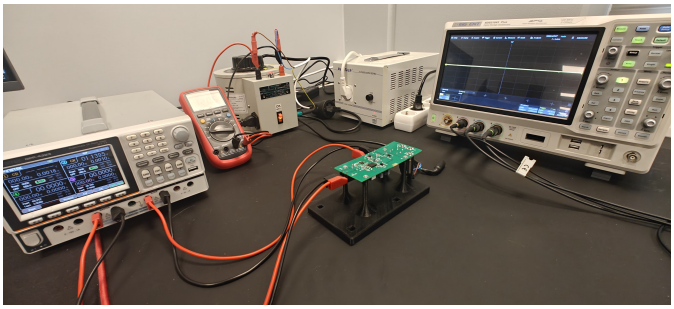


Figure 4.1.5: Power supply connected to the test setup.

Unfortunately, the power supply did not produce the desired voltages regardless of the presence of load on the outputs or not. The input voltage war varied between 85-265VAC but this had no effect on the output. This started a long journey of troubleshooting in order to identify the issue.
This process of troubleshooting is not well documented, due to the lack of time and the focus being getting the power supply to function correctly. Nonetheless, here is a summary of this process:

- Measurements of relevant test points were made They were as expected on the primary side, but was zero or much lower than expected on the secondary side. This suggests that the PMIC is either not starting at all or going into auto restart.
- To eliminate the possibility of faulty components or bad soldering, another PCB sample was mounted, but it produced exactly the same results.
- To verify that the PMIC was attempting to switch the primary FET, the drain voltage was measured. Figure 4.1.6 shows the oscilloscope images for this measurement.

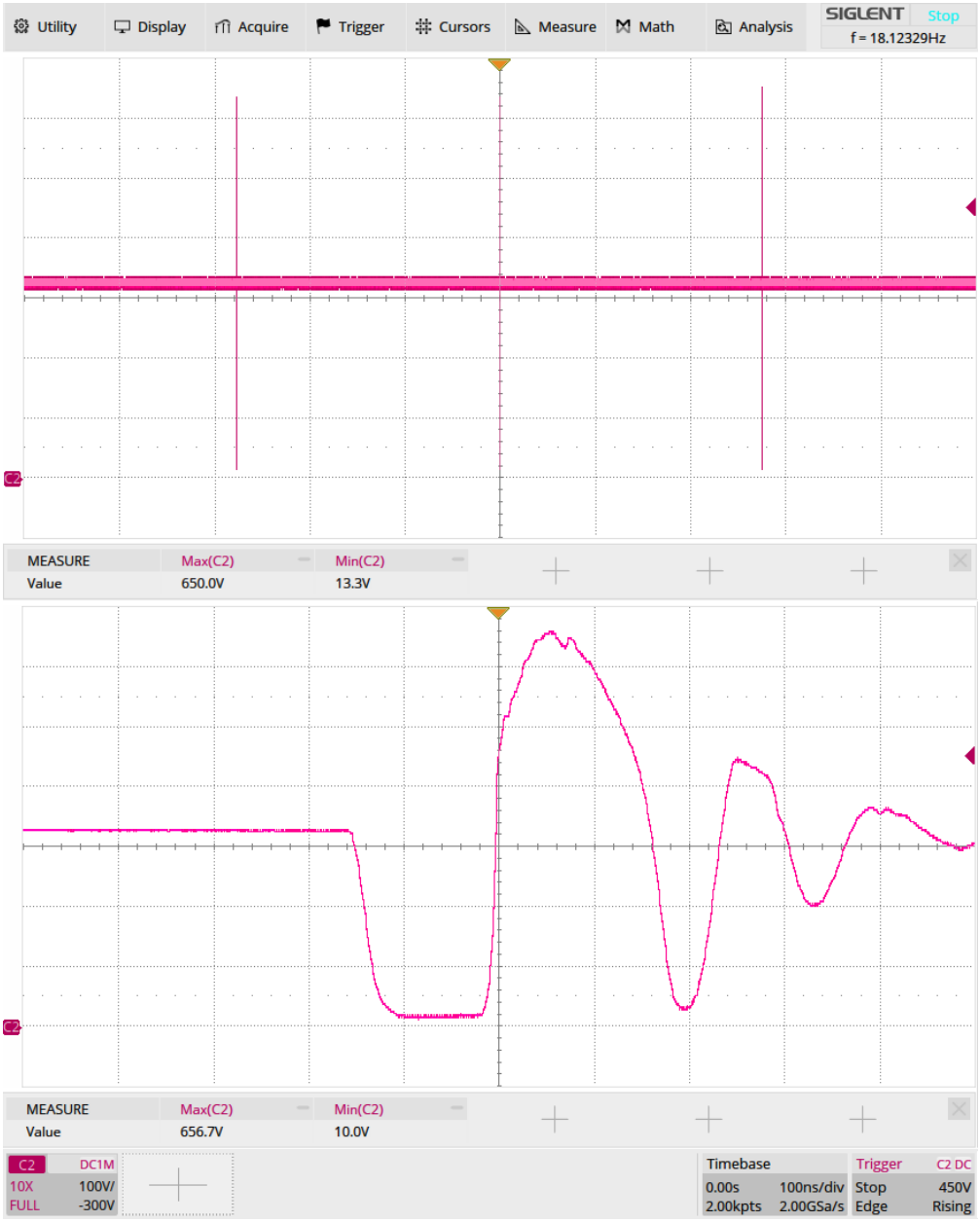
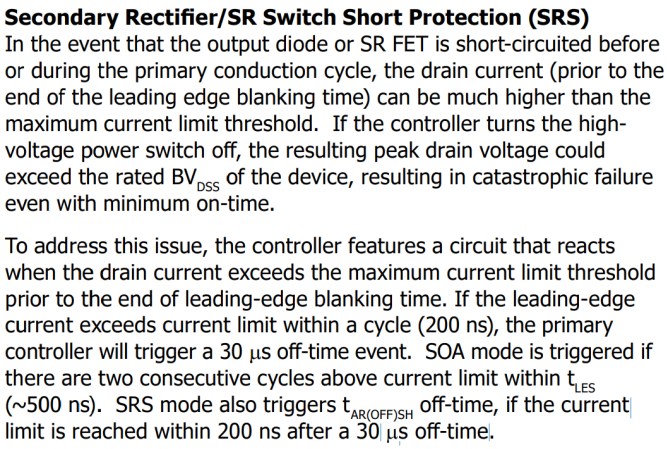


Figure 4.1.6: Drain voltage measurements.

It seems that the PMIC is switching on the FET for about 100 ns and then turn it off again, wait for around 230 ms and tries again. This points in the direction that one of the protections is being triggered.

- The protections that the PMIC have are: line over and undervoltage protection, output overvoltage and over-current limiting, and over-temperature shutdown. Measurements were made to confirm that it it not line over and undervoltage protection or over-temperature shutdown. It can not be output overvoltage limiting as the voltage is non-existent on the output. The over-current limiting was not logical either as there the current should be very small.

- Digging deeper into the Innoswitch3-ep family datasheet, it states that the normal auto-restart off-time is between 1.7 and 2.11 second. There is also short auto-restart off-time between 0.17 and 0.23 second. The short auto-restart off-time is exactly what have been measured earlier. This time is mentioned again in the datasheet again only once in the paragraph "Secondary Rectifier/SR Switch Short Protection (SRS)" on page 5 [8]. Figure 4.1.7 shows this paragraph.



Secondary Rectifier/SR Switch Short Protection (SRS)
In the event that the output diode or SR FET is short-circuited before or during the primary conduction cycle, the drain current (prior to the end of the leading edge blanking time) can be much higher than the maximum current limit threshold. If the controller turns the high-voltage power switch off, the resulting peak drain voltage could exceed the rated BV_{DSS} of the device, resulting in catastrophic failure even with minimum on-time.

To address this issue, the controller features a circuit that reacts when the drain current exceeds the maximum current limit threshold prior to the end of leading-edge blanking time. If the leading-edge current exceeds current limit within a cycle (200 ns), the primary controller will trigger a 30 µs off-time event. SOA mode is triggered if there are two consecutive cycles above current limit within t_{LES} (~500 ns). SRS mode also triggers $t_{AR(OFF)SH}$ off-time, if the current limit is reached within 200 ns after a 30 µs off-time.

Figure 4.1.7: Secondary Rectifier/SR Switch Short Protection (SRS).

- To confirm that the drain current is exceeding the maximum current limit threshold, the board was modified as shown in figure 4.1.8 in order to make it possible to use a current clamp to measure the drain current.

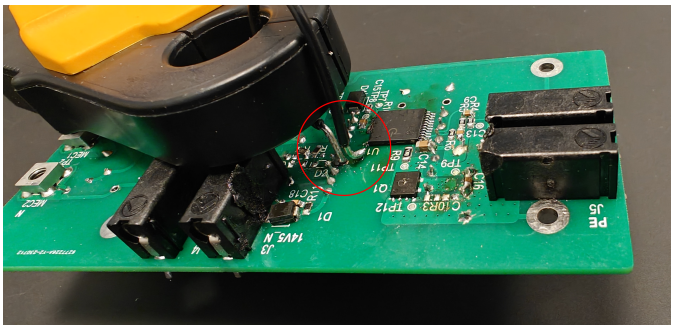


Figure 4.1.8: Board modification in order to measure drain current.

Figure 4.1.9 shows the oscilloscope image for this measurement. The current spike is measured at 11.17 A with no load on the outputs, this is a lot higher than the maximum current limit threshold. Lowering the input voltage lowered this spike, but not enough to allow the PMIC to start-up.

Figure 4.1.9: Drain current spike measurements.

- As there is no short circuit on the secondary side, there must be another reason why the drain current spike is exceeding the maximum current limit threshold. This turned out to be a common problem with Flyback converters where the reverse recovery current from the secondary rectifier flows back into the primary winding, causing a spike in the primary current (drain current), when the primary FET turns on [7].

- Removing only D1 (secondary rectifier for output2) from the board, allowed the power supply to function albeit at up to 110VAC input voltage.

- Reverse recovery time is closely related to junction capacitance on diodes and to output capacitance on MOSFETs. Taking a closer look at the components used in the design, the secondary diodes D1 and D2 (vssb420s-m3) have 120 pF junction capacitance each and the secondary MOSFET (DMT10H009SPS) has output capacitance 609 pF. These values are quite high, in addition to the other parasitics like the transformer parasitics has caused the high leading edge current spike and prevented the power supply from functioning.

- Components with better characteristics were ordered.
  Several Schottky diodes with lower junction capacitance, they did not improve the situation. This might be caused by the fact that Schottky diodes has very fast reverse recovery time such that regardless of how small the junction capacitance is, they would still cause a very high current spike.
  However, when the snubber diode (RS07K-GS08) with a junction capacitance of just 4 pF and relatively slow reverse recovery time of 300 ns, was used instead of the Schottky, this allowed the power supply to function albeit at up to 170VAC input voltage.
  Secondary MOSFET was replaced with (BSC440N10NS3 G) which har much lower output capacitance at 120 pF. This was far more successful and allowed the power supply to function albeit at up to 265VAC input voltage at full load on output1.

- Another method to solve this problem would be to use the PMIC H605 variant that has "Secondary Rectifier/SR Switch Short Protection (SRS)" disabled. This will not be ideal as such a high current spike might destroy the primary FET.

- The potential issue with the lack of feedback from the second output was present as previously predicted in the simulation shown in figure 3.1.2, this prevented the power supply from starting up most of the time. Even when it managed to start up at certain load conditions, it shut down at some point when the load change was too big. Also the voltage on the second output was very badly regulated. This should be solvable relatively easily by adding a feedback from the second output using an optocoupler.

4.2 Preliminary performance tests

Although the power supply could not function correctly with both outputs as originally designed, performing some key measurements and running some performance tests is still valuable. Due to the large amount of time spent on troubleshooting the power supply, not all the desired tests were possible to conduct within the time-frame of this work.

4.2.1 Line regulation

This evaluate the power supply to maintain the output voltage under different input voltage levels, these measurements were done at 1.62 A. The results are presented in this table 4.2.1 and plotted in this figure 4.2.1. The plot shows that the power supply struggles at lower input voltage but it still manages to keep the output voltage at an acceptable level.

Input Voltage (VAC)	85	115	130	180	230	265	279
Output 1 Voltage (14.5 V)	14.21	14.47	14.46	14.55	14.61	14.61	14.62

Table 4.2.1: Line regulation.

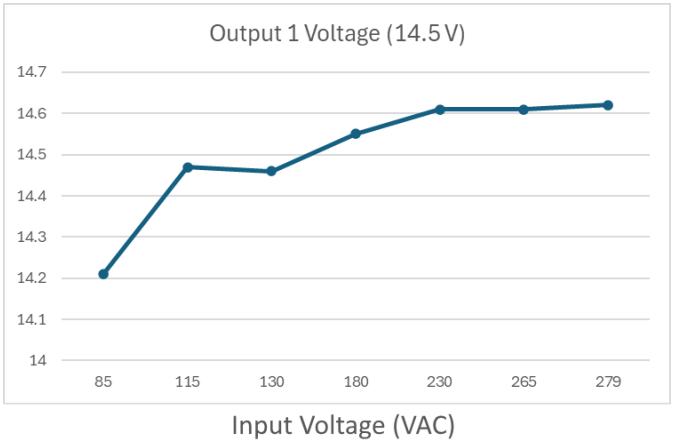


Figure 4.2.1: Line regulation.

4.2.2 Switching waveforms

These measurements were done at 230 VAC 50 Hz, 1.62 A. Figure 4.2.2 and figure 4.2.3 show primary MOSFET drain-source voltage at normal operation and at start-up respectively. Figure 4.2.4 and figure 4.2.5 show output 1 synchronous rectifier voltage at normal operation and at start-up respectively.

Figure 4.2.2: Primary MOSFET drain-source voltage at normal operation.

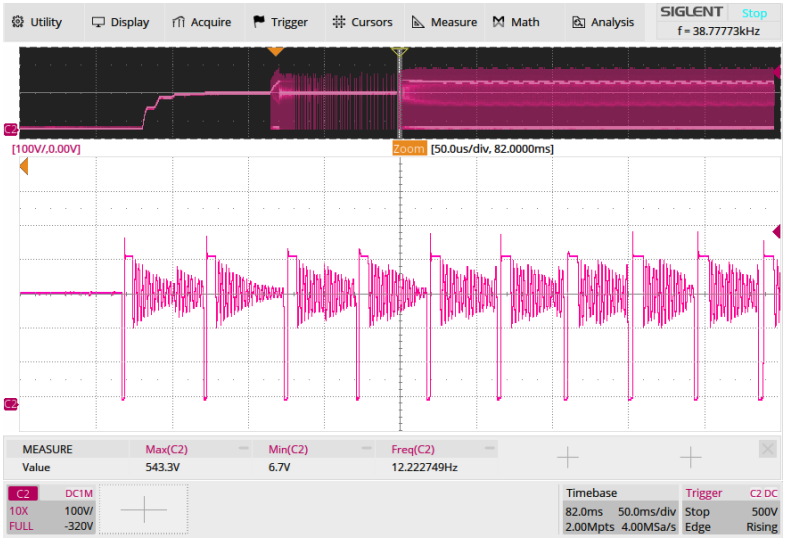


Figure 4.2.3: Primary MOSFET drain-source voltage at start-up.

The previous figures show that the primary MOSFET does not experience any voltage higher than 550 V during start-up or normal operation, this gives a good margin from the 725 V breakdown voltage. This suggests that the snubber values are suitable and do not need adjustment. The switching frequency during normal operation is around 46 kHz which is lower than the target frequency of 65 kHz, this is also a healthy margin.

Figure 4.2.4: Synchronous rectifier voltage at normal operation.

Figure 4.2.5: Synchronous rectifier voltage at start-up.

The previous figures show that the synchronous rectifier MOSFET does not experience any voltage higher than 75 V during start-up or normal operation, this gives a good margin from the 100 V breakdown voltage. This suggests that the snubber values are suitable and do not need adjustment. The switching frequency during normal operation is also around 46 kHz,

this is the same frequency observed on the primary side as expected.
The resonance frequency is measured at 469 kHz shown in figure 4.2.4, using the equation 2.11 we get a parasitic capacitance for the transformer of 78 pF which is very close to the measured parasitic capacitance between Primary winding and Bias winding in transformer parasitics measurements section 4.1.2.

4.2.3 Efficiency

These measurements were done at 230 VAC 50 Hz, 1.62 A being the 100% load level. The results are presented in this table 4.2.2 and plotted in this figure 4.2.6. These results were quite surprising as the best efficiency was around 60%, this suggests a mistake in the measurement method or some design mistake. In addition the no load power consumption was measured at 1.77 W, this is very high as it is expected to be around 40 mW. This needs to be investigated further.

Percentage Load (%)	5	10	20	50	100
PIN (W)	3.749	5.842	9.522	21.045	40.25
POUT (W)	1.16	2.33	4.68	11.88	23.92
Efficiency (%)	0.309415844	0.398836	0.491493	0.564505	0.594286

Table 4.2.2: Efficiency at different Percentage loads

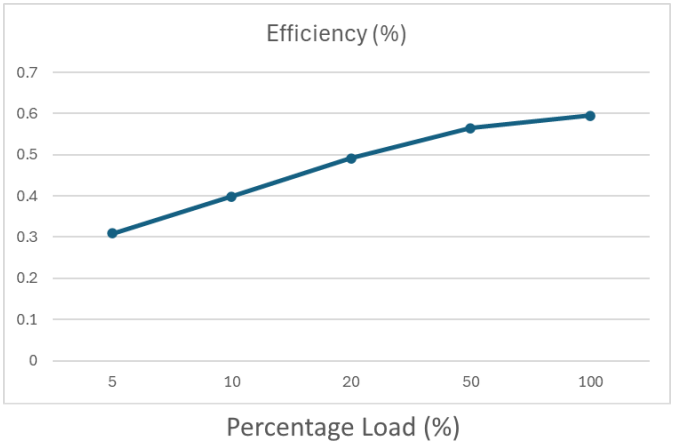


Figure 4.2.6: Efficiency at different Percentage loads.

4.2.4 Output ripple measurement

These measurements were done at 230 VAC 50 Hz, 1.62 A. Figure 4.2.7 shows ripple voltage on output 1. Ignoring the high frequency spikes, gives an output ripple around 130 mV. This is 0.9 % of the output voltage, this is a very good result. Taking the high frequency spikes into consideration, gives an output ripple around 733 mV. This is 5 % of the output voltage, which is still acceptable. It is also observed that the fusible resistor is somewhat hotter than the other component, this potentially points at this component as the source of the losses and the unexpected low efficiency of the power supply.

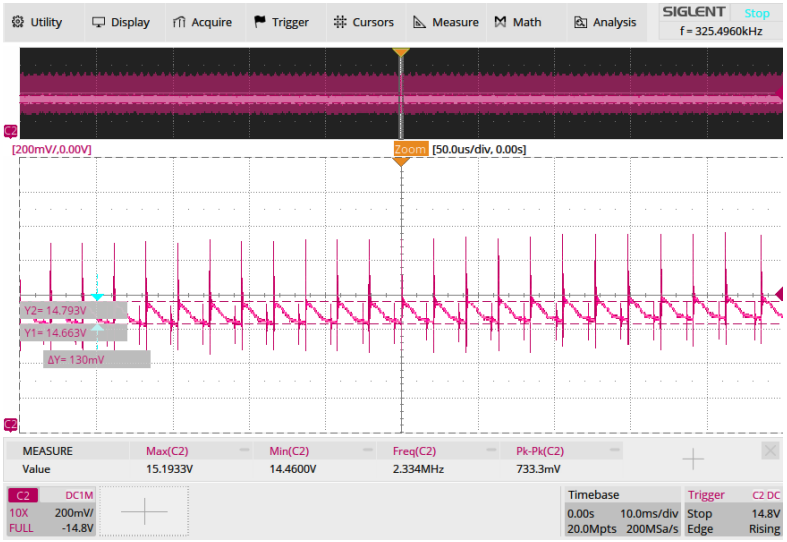


Figure 4.2.7: Output ripple measurement.

4.2.5 Thermal performance

These images were taken at 230 VAC 50 Hz, 1.62 A after 30 minutes under load. Figure 4.2.8 and figure 4.2.9 show the temperature of the various components on the top and bottom of the power supply. The images were taken with a low resolution thermal camera, nonetheless it is possible to see that the temperatures are reasonable. It is also observed that the fusible resistor and the transformer are somewhat hotter than the other component, this potentially points at these components might be the source of the losses and the unexpected low efficiency of the power supply. The voltage drop over the fusible resistor was ca. 6.15 V and thus a loss of about 1.17 W, this is too low to explain the lack of efficiency on its own.

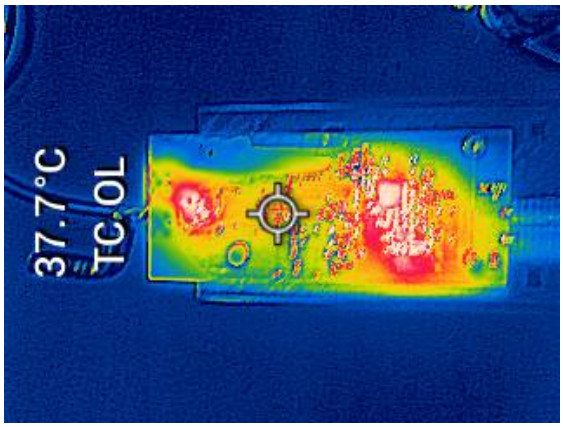


Figure 4.2.8: Thermal image bottom.

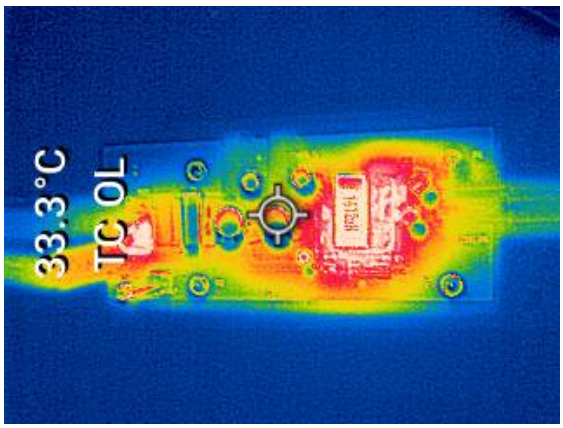


Figure 4.2.9: Thermal image top.

4.3 Discussion

The power supply worked partially after considerable amount of troubleshooting, only with one output active and the efficiency was way less than desired (measured 60% vs desired 85%). Regarding hardware design, the produced circuit had some design mistakes, the lack of feedback from the second output and usage of unsuitable components resulted in the previously discussed leading edge current spike. Regarding production and soldering, this went well

without any challenges. Regarding testing, it is possible that the hardware design contains other mistakes that have not been discovered due to the limited amount of testing, but it can be concluded that the design is functional. Better testing procedures should have been followed.

A combination of mistakes and challenges lead to none-optimal results, these are listed here:

- The goals for this work were ambitious to begin with, and got further derailed by the unexpected start-up issue.
- Most of the work has been done independently, resulting in prolonged time of researching issues and trial and error.
- The classic mistake of doing tests during development and not documenting them was made.

Key highlights of this work are listed here:

- Most of the work has been done independently. This was intentional as developing competence on the topic of power supplies is one of the goals of this work, as researching topics on your own gives more dividends than being handed the answers.
- Limiting the scope of this work by using an integrated solution as a base for the design, helped achieve partial success.
- Being meticulous with schematic and layout design, taking into consideration production methods in advance and following guidelines and standards, resulted in a smooth production process.

4.3.1 Further development

The following areas require more work:

- Implement the optocoupler feedback circuit and obtain a fully functioning dual output Flyback converter.
- Investigate the low efficiency of the converter and improve it.
- Perform a more comprehensive suite of tests as originally planed, including EMI and ESD tests.

Chapter 5

Conclusion

Although the project fell short of the goalpost, it still produced a partially functioning prototype that can be iterated on and improved. A considerable amount of experience and competence in the topic of power supply design, building, and troubleshooting was obtained. Several of the performed tests produced the expected results, while mainly the efficiency measurement requires further investigation. The validity of the basic design and its ability to satisfy the desired specifications of the power supply were proved. The use of an integrated PMIC solution showed the expected advantages of simplicity and reduction of component count, as well as the drawbacks of lack of control over the specifics of the implemented circuits and algorithms.

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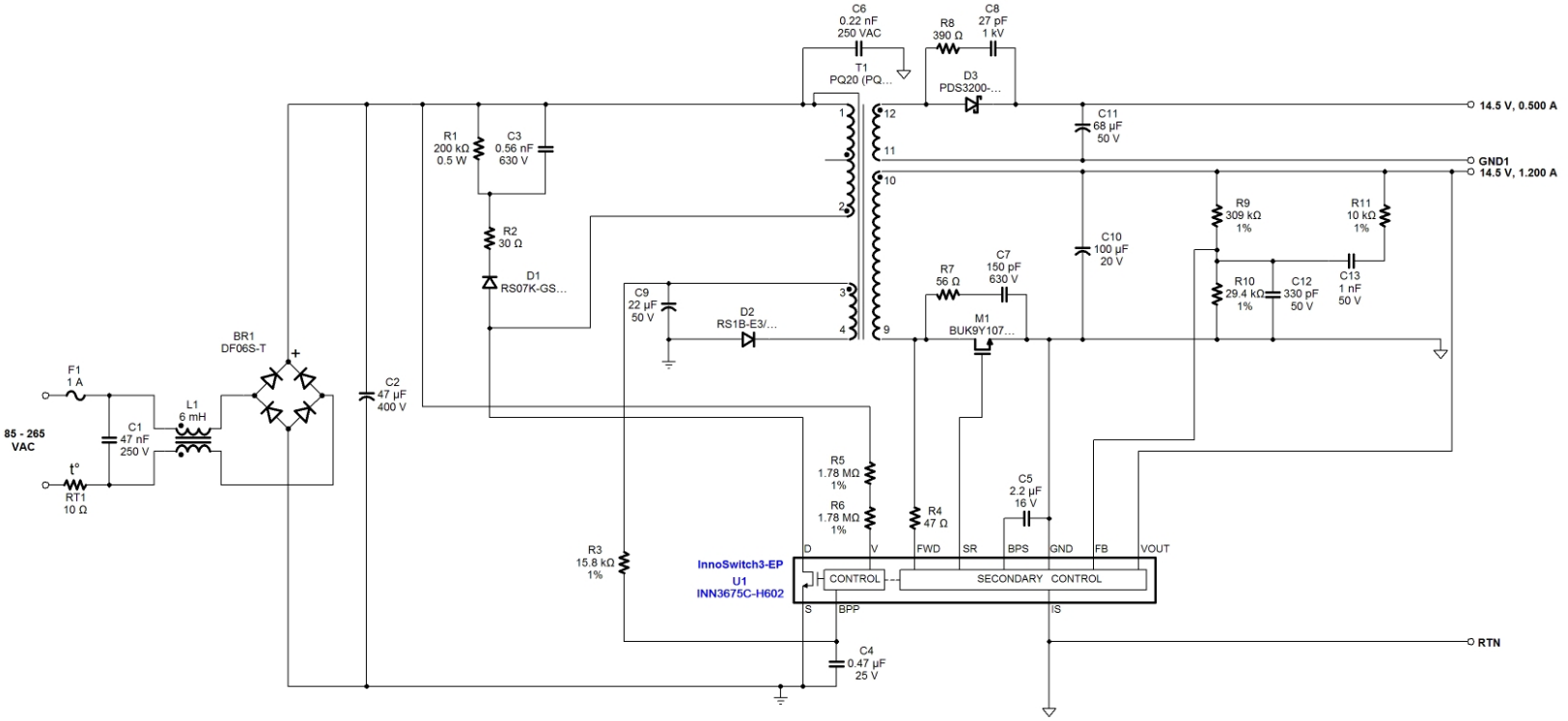
Appendix A

PI expert design

This appendix includes the design outputs from PI expert software.



Schematic components that have been frozen by the user will appear with blue reference designators.

For any information regarding user added Shield or Screen and additional EMI features implemented in the Transformer, review Magnetics Designer.

Power Supply Input

Var	Value	Units	Description
VACMIN	85	V	Minimum Input AC Voltage
VACNOM	115	V	Nominal AC Voltage (For universal designs low line nominal voltage is displayed)
VACMAX	265	V	Maximum Input AC Voltage
FL	50	Hz	Line Frequency
η	87.0	%	Efficiency Estimate (Target)
TC	2.71	ms	Input Rectifier Conduction Time
Z	0.50		Loss Allocation Factor
VMIN	78.2	V	Minimum DC Input Voltage
VMAX	374.8	V	Maximum DC Input Voltage
ENCLOSURE	Adapter		Enclosure (Manual Overwrite)
TAMB	70	°C	Maximum Operating Ambient air Temperature (Manual Overwrite)

Input Section

Var	Value	Units	Description
Fuse	1.00	A	Input Fuse Rated Current
IAVG	0.34	A	Average Diode Bridge Current (DC Input Current)
Thermistor	10.00	Ω	Input Thermistor

Device Variables

Var	Value	Units	Description
Device	INN3675C-H602		PI Device Name (Manual Overwrite). See Information section for detail
Current Limit Mode	Standard		Device Current Limit Mode
BVDSS	725	V	Drn-Src Bkdn Voltage
ILIMITMIN	0.883	A	Minimum Current Limit
ILIMITTYP	0.950	A	Typical Current Limit
ILIMITMAX	1.016	A	Maximum Current Limit
RDSON	3.02	Ω	PI Device RDSON (100°C)
RDSON_25C	1.95	Ω	PI Device RDSON (25°C)
PO	24.65	W	Total Output Power
VOR	109.66	V	Reflected Output Voltage
VDS	1.04	V	On state Drain to Source Voltage
FS	65000	Hz	Switching Frequency (at VMIN and Full Load) (Manual Overwrite)
KP	0.590		Continuous/Discontinuous Operating Ratio (at VMIN and Full Load)
DMAX	0.587		Maximum Duty Cycle (at VMIN and Full Load)
TIME_OFF	6.36	µs	Expected Device Off-time (at VMIN and Full Load)
TIME_ON	14.92	µs	Primary controller on-time
IP	0.918	A	Peak Primary Current (at VMIN and Full Load)
IR	0.666	A	Primary Ripple Current (at VMIN and Full Load)

IRMS	**0.472**	*A*	*Primary RMS Current (at VMIN and Full Load)*
UVOV_PRIORITY	**Overvoltage**		*Input Undervoltage/Overvoltage Priority type*
RTH_DEVICE	**60.30**	*°C/W*	*PI Device Heatsink Maximum Thermal Resistance*
DEV_HSINK_TYPE	**2 Oz (70 µ) 2-Sided Copper PCB**		*PI Device Heatsink Type*
DEV_HSINK_AREA	**397**	*mm²*	*PI Device Heatsink Area*

Clamp Circuit

Var	*Value*	*Units*	*Description*
Clamp Type	**RCD Clamp**		*Clamp Circuit Type*
VCLAMP_ESTIMATED	**271.35**	*V*	*Estimated Clamping Voltage above VMAX*
VDRAIN Estimated	**646.12**	*V*	*Estimated Drain Voltage*

Primary Bias Variables

Var	*Value*	*Units*	*Description*
VBMIN	**12.5**	*V*	*Minimum Bias Voltage*
VBMAX	**32.0**	*V*	*Maximum Bias Voltage*
Circuit Type	**Simple Resistor**		*Bias Circuit Type*
PIVB	**81**	*V*	*Bias Rectifier Maximum Peak Inverse Voltage*
NB	**10**		*Primary Bias Winding Number of Turns*

Transformer Construction Parameters

Var	*Value*	*Units*	*Description*
Core Type	**PQ20 (PQ20/16-3F3)**		*Core Type*
Core Material	**3F3**		*Core Material (Manual Overwrite)*
LP_nom	**1448**	*µH*	*Nominal Primary Inductance*
LP_Tol	**5.0**	*%*	*Primary Inductance Tolerance*
NP	**76.0**		*Calculated Primary Winding Total Number of Turns*
NSM	**10**		*Secondary Main Number of Turns (Manual Overwrite)*
Primary Current Density	**9.54**	*A/mm²*	*Primary Winding Current Density*
BW	**7.82**	*mm*	*Bobbin Winding Width*
FF	**62.40**	*%*	*Actual Transformer Fit Factor. 100% signifies fully utilized winding window*
AE	**61.90**	*mm²*	*Core Cross Sectional Area*
ALG	**251**	*nH/T²*	*Gapped Core Specific Inductance*
BM	**292**	*mT*	*Maximum Flux Density*
BP	**336**	*mT*	*Peak Flux Density*
BAC	**146**	*mT*	*AC Flux Density for Core Loss*
LG	**0.285**	*mm*	*Estimated Gap Length*
L_LKG	**16.32**	*µH*	*Estimated primary leakage inductance*
LSEC	**20**	*nH*	*Secondary Trace Inductance*

Primary Winding Section 1

Var	*Value*	*Units*	*Description*
NP1	**51**		*Number of Primary Winding Turns in the First Section of Primary*

L	**2.00**		*Primary Winding - Number of Layers*

Primary Winding Section 2

Var	*Value*	*Units*	*Description*
NP2	**25**		*Rounded (Integer) Number of Primary winding turns in the second section of primary*
L2	**1.00**		*Primary Number of Layers in 2nd split winding*

Output 1

Var	*Value*	*Units*	*Description*
VO	**14.50**	*V*	*Typical Output Voltage*
IO	**1.200**	*A*	*Output Current*
VOUT_ACTUAL	**14.50**	*V*	*Actual Output Voltage*
Cable Drop Compensation	**0**	*mV*	*Cable Drop Compensation*
NS	**10**		*Secondary Number of Turns*
L_S_OUT	**1.00**		*Secondary Output Winding Layers*
PIVS	**63.81**	*V*	*Output Rectifier Maximum Peak Inverse Voltage*
ISP	**4.923**	*A*	*Peak Secondary Current*
ISRMS	**2.123**	*A*	*Secondary RMS Current*
ISRMS_WINDING	**2.123**	*A*	*Secondary Winding RMS Current*
Secondary Current Density	**11**	*A/mm²*	*Secondary Winding Current Density*
RTH_RECTIFIER	**45.60**	*°C/W*	*Output Rectifier Heatsink Maximum Thermal Resistance*
OR_HSINK_TYPE	**2 Oz (70 µ) 2-Sided Copper PCB**		*Output Rectifier Heatsink Type*
OR_HSINK_AREA	**276**	*mm²*	*Output Rectifier Heatsink Area*
OSR_RDSON	**107.00**	*mΩ*	*Synchronous Rectifier RDSON*
CO	**100 x 1**	*µF*	*Output Capacitor - Capacitance*
IRIPPLE	**1.751**	*A*	*Output Capacitor - RMS Ripple Current*
Expected Lifetime	**13452**	*hr*	*Output Capacitor - Expected Lifetime*

Output 2

Var	*Value*	*Units*	*Description*
VO	**14.50**	*V*	*Typical Output Voltage*
IO	**0.500**	*A*	*Output Current*
VOUT_ACTUAL	**15.17**	*V*	*Actual Output Voltage*
Cable Drop Compensation	**0**	*mV*	*Cable Drop Compensation*
NS	**11**		*Secondary Number of Turns*
L_S_OUT	**1.00**		*Secondary Output Winding Layers*
VD	**0.78**	*V*	*Output Winding Diode Forward Voltage Drop*
PIVS	**69.41**	*V*	*Output Rectifier Maximum Peak Inverse Voltage*
ISP	**2.051**	*A*	*Peak Secondary Current*
ISRMS	**0.884**	*A*	*Secondary RMS Current*
ISRMS_WINDING	**0.884**	*A*	*Secondary Winding RMS Current*
Secondary Current Density	**6**	*A/mm²*	*Secondary Winding Current Density*
RTH_RECTIFIER	**76.64**	*°C/W*	*Output Rectifier Heatsink Maximum Thermal Resistance*

OR_HSINK_TYPE	**2 Oz (70 µ) 2-Sided Copper PCB**		*Output Rectifier Heatsink Type*
OR_HSINK_AREA	**104**	*mm²*	*Output Rectifier Heatsink Area*
CO	**68 x 1**	*µF*	*Output Capacitor - Capacitance*
IRIPPLE	**0.730**	*A*	*Output Capacitor - RMS Ripple Current*
Expected Lifetime	**59688**	*hr*	*Output Capacitor - Expected Lifetime*

Feedback Circuit

Var	*Value*	*Units*	*Description*
DUAL_OUTPUT_FB_FLAG	**NO**		*Get feedback from 2 outputs*

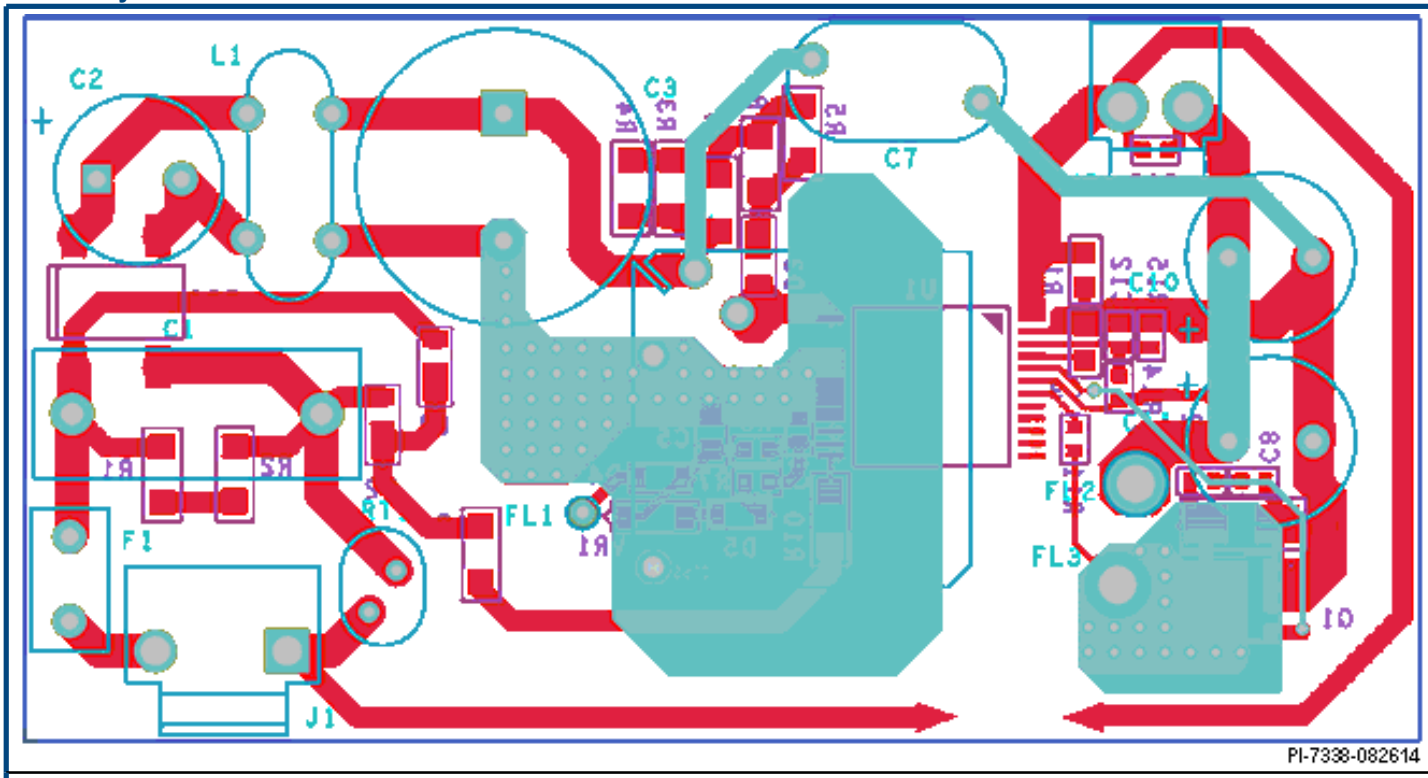
Power Supply Efficiency and Losses (at VACMIN - VACNOM and Full Load)

Var	*Value*	*Units*	*Description*
N_ACTUAL_RANGE	**83.76-85.38**	*%*	*Calculated Efficiency*
TOTAL_LOSS_RANGE	**4.22-4.78**	*W*	*Total Power Supply Losses*
DEV_LOSS_RANGE	**0.68-0.70**	*W*	*Total Device Circuit Losses*
TRF_LOSS_RANGE	**0.67-0.78**	*W*	*Total Transformer Losses*
INSTAGE_LOSS_RANGE	**1.11-1.49**	*W*	*Total Primary Side Losses*
OUTSTAGE_LOSS_RANGE	**1.76-1.84**	*W*	*Total Secondary Side Losses*

The regulation and tolerances do not account for thermal drifting and component tolerance of the output diode forward voltage drop and voltage drops across the LC post filter. The actual voltage values are estimated at full load only.

Please verify cross regulation performance on the bench.

Board Layout Recommendations



Click on the "Show me" icon to highlight relevant areas on the sample layout.

	Description	Show Me
1	*Minimize loop area formed by secondary winding, the output rectifier and the output filter capacitor*	
2	*Y-capacitor connected directly to the DC pin of the primary and secondary GND*	
3	*Minimize loop area formed by drain, clamp and transformer*	
4	*Maximize hatched area for heat-sinking*	
5	*Minimize loop area formed by drain, input capacitor and transformer*	
6	*Spark gaps with adequate creepage help in steering away the destructive energy created during an ESD event through the protection components such as the Y-cap.*	
7	*The BYPASS pin capacitor should be located as close as possible to the BYPASS and SOURCE pins*	

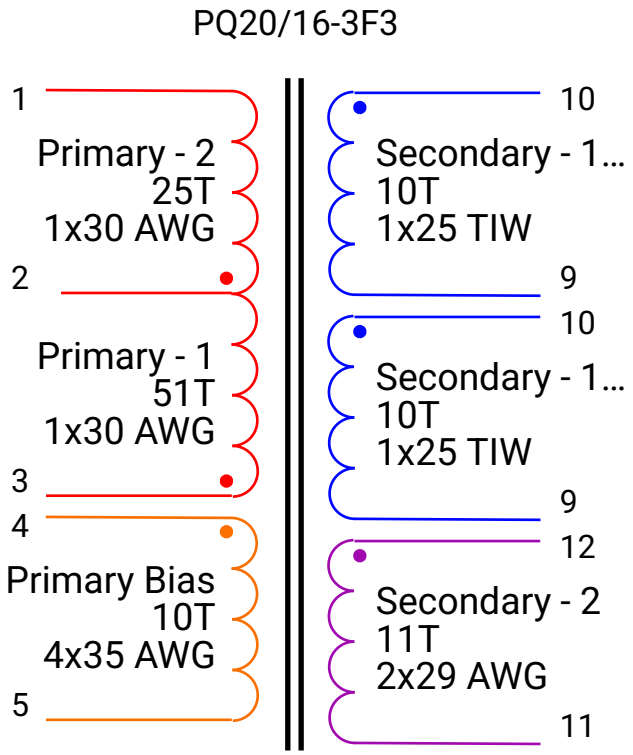
Bill Of Materials

Item #	Quantity	Part Ref	Value	Description	Mfg	Mfg Part Number
1	1	BR1	DF06S-T	600 V, 1 A, Standard Recovery Bridge, DFS	Diodes Inc.	DF06S-T
2	1	C1	47 nF	47 nF, 250 V, Film, X Class	Murata	GA355ER7GB473KW01L
3	1	C2	47 µF	47 µF, 400 V, High Voltage Al Electrolytic, (25 mm x 22 mm)	Cornell Dubilier	381LX470M400H012
4	1	C3	0.56 nF	0.56 nF, 630 V, High Voltage Ceramic	Murata	GRM31A5C2J561JW01D
5	1	C4	0.47 µF	0.47 µF, 25 V, Ceramic, X7R	Kemet	C0805C474K3RAC7800
6	1	C5	2.2 µF	2.2 µF, 16 V, Ceramic, X7R	TDK	CGA4J3X7R1C225K125AB
7	1	C6	0.22 nF	0.22 nF, 250 VAC, Ceramic, Y Class	Vishay	VJ2008A221JXUSTX1
8	1	C7	150 pF	150 pF, 630 V, High Voltage Ceramic	TDK	C3216C0G2J151J060AA
9	1	C8	27 pF	27 pF, 1 kV, High Voltage Ceramic	Murata	GRM31A5C3A270JW01D
10	1	C9	22 µF	22 µF, 50 V, Electrolytic, Gen Purpose, 80 mΩ, (6.3 mm x 5.8 mm)	Panasonic	EEHZC1H220P
11	1	C10	100 µF	100 µF, 20 V, Al Organic Polymer, 20 mΩ, (10 mm x 10 mm)	Wurth Elektronik	875115452003
12	1	C11	68 µF	68 µF, 50 V, Al Organic Polymer, 32 mΩ, (12 mm x 10 mm)	Kemet	A759MS686M1HAAE032
13	1	C12	330 pF	330 pF, 50 V, Ceramic, C0G	TDK	FK18C0G1H331J
14	1	C13	1 nF	1 nF, 50 V, Ceramic, C0G	Kemet	C410C102J5G5TA7200
15	1	D1	RS07K-GS08	800 V, 1.4 A, Fast Recovery, 300 ns, DO-219AB	Vishay	RS07K-GS08
16	1	D2	RS1B-E3/61T	100 V, 1 A, Standard Recovery, DO-214AC	Vishay	RS1B-E3/61T
17	1	D3	PDS3200-13	200 V, 3 A, Schottky, PowerDI-5	Diodes Inc.	PDS3200-13
18	1	F1	1 A	250 VAC, 1 A, Radial TR5, Time Lag Fuse	Littelfuse / Wickmann(R)	37411000410
19	1	L1	6 mH	6 mH, 1.6 A	Panasonic	ELF18N016
20	1	M1	BUK9Y107-80EX	MOSFET, N-Channel, 80 V, 8.3 A, SOT669	Nexperia	BUK9Y107-80EX
21	1	R1	200 kΩ	200 kΩ, 5 %, 0.5 W, Thick Film	Generic	
22	1	R2	30 Ω	30 Ω, 5 %, 0.125 W, Thick Film	Generic	
23	1	R3	15.8 kΩ	15.8 kΩ, 1 %, 0.125 W, Thick Film	Generic	
24	1	R4	47 Ω	47 Ω, 5 %, 0.125 W, Thick Film	Generic	
25	2	R5, R6	1.78 MΩ	1.78 MΩ, 1 %, 0.25 W, Thick Film	Generic	
26	1	R7	56 Ω	56 Ω, 5 %, 0.25 W, Thick Film	Generic	
27	1	R8	390 Ω	390 Ω, 5 %, 0.25 W, Thick Film	Generic	
28	1	R9	309 kΩ	309 kΩ, 1 %, 0.125 W, Thick Film	Generic	
29	1	R10	29.4 kΩ	29.4 kΩ, 1 %, 0.125 W, Thick Film	Generic	
30	1	R11	10 kΩ	10 kΩ, 1 %, 0.125 W, Thick Film	Generic	
31	1	RT1	10 Ω	NTC Thermistor 10 Ω, 1.7 A	Thermometrics	CL-120

32	1	T1	PQ20 (PQ20/16-3F3)	3F3 Core Material Refer to Manufacturer datasheet for a number of parts to purchase	Ferroxcube	PQ20/16-3F3
33	1	T1 Bobbin	PQ20/16 - 1 (P8-S6)	Bobbin Material : Thermoplastic polyester	Ferroxcube	CPV-PQ20/16-1S-14P
34	1	T1 Core Acc.1	CLM/P-PQ20/26	Clamp . Phosphorbronze, Sn plated	Ferroxcube	CLM/P-PQ20/26
35	1	U1	INN3675C-H602	InnoSwitch3-EP, INN3675C-H602, inSOP-24D	Power Integrations	INN3675C-H602
36	1			1182 mm² area on Copper PCB. 2 oz (70 µm) thickness. Heatsink for use with Device U1.	Custom	
37	1			355 mm² area on Copper PCB. 2 oz (70 µm) thickness. Heatsink for use with Rectifier M1.	Custom	
38	1			104 mm² area on Copper PCB. 2 oz (70 µm) thickness. Heatsink for use with Rectifier D3.	Custom	

TRANSFORMER CONSTRUCTION REPORT

Electrical Diagram



Winding info

Stack Fill Factor: 70.35%;
Total Copper Weight: 3.54g
Copper Loss: 0.373W; Total Transformer Loss: 0.462W

8.33%H; Primary - 2; IRMS = 0.27A;
1L; 25T; 1x30 AWG; CMA = 365.04 Cmils/A; LENw = 128.2 cm;
RDC = 574.32 mΩ; RAC = 581.41 mΩ; WeightCU = 0.58 g; Pw = 43.66 mW;

9.3%H; Secondary - 2; IRMS = 0.87A;
0.96L; 11T; 2x29 AWG; CMA = 293.98 Cmils/A; LENw = 54.2 cm;
RDC = 95.07 mΩ; RAC = 97.25 mΩ; WeightCU = 0.63 g; Pw = 76.55 mW;

16.3%H; Secondary - 1 - 2; IRMS = 1.4A;
1L; 10T; 1x25 TIW; CMA = 229.07 Cmils/A; LENw = 46.2 cm;
RDC = 64.45 mΩ; RAC = 69.64 mΩ; WeightCU = 0.67 g; Pw = 82.73 mW;

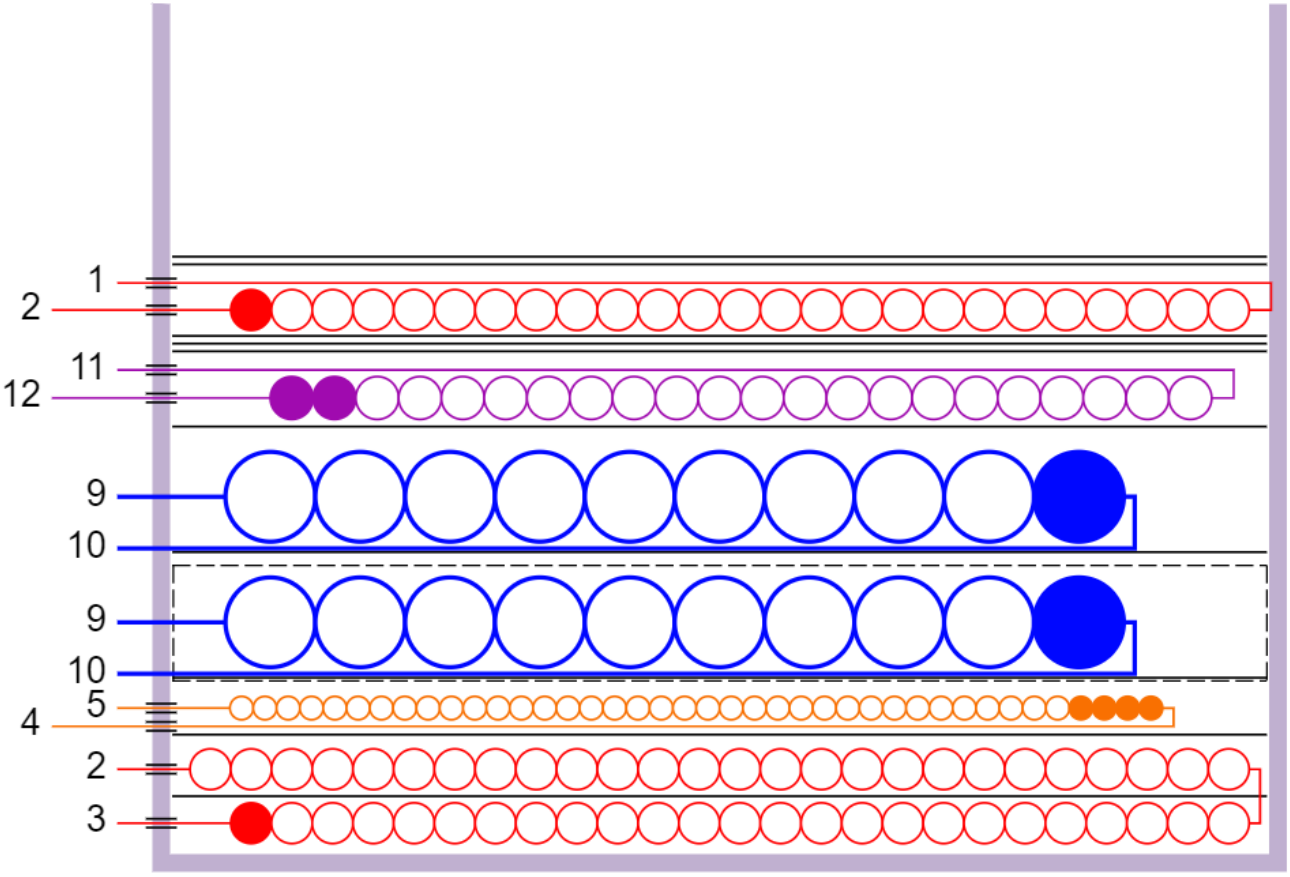
16.3%H; Secondary - 1 - 1; IRMS = 1.54A;
1L; 10T; 1x25 TIW; CMA = 207.86 Cmils/A; LENw = 41.9 cm;
RDC = 58.48 mΩ; RAC = 63.18 mΩ; WeightCU = 0.61 g; Pw = 75.15 mW;

4.68%H; Primary Bias; IRMS = 0.01A;
0.96L; 10T; 4x35 AWG; LENw = 39.2 cm;

15.44%H; Primary - 1; IRMS = 0.27A;
2L; 51T; 1x30 AWG; CMA = 365.04 Cmils/A; LENw = 183.1 cm;
RDC = 820.05 mΩ; RAC = 870.27 mΩ; WeightCU = 0.83 g; Pw = 95.35 mW;

All losses shown correspond to the nominal current limit and primary winding inductance at the minimum AC voltage.

Mechanical Diagram


1
2
11
12
9
10
9
10
5
4
2
3

Building Instructions

LIST OF MATERIALS

Item	Description
[1]	Core: PQ20/16-3F3, 3F3, gapped for ALG of 211 nH / T^2
[2]	Bobbin: Thermoplastic polyester CPV-PQ20/16-1S-14P
[3]	Teflon Tubing # 22
[4]	Varnish
[5]	Single core wire: 30 AWG (0.3 mm), insulation Heavy Build
[6]	Separation Tape: Polyester film [1 mil (25.4 micrometers) base thickness], 7.82 mm wide
[7]	Single core wire: 35 AWG (0.17 mm), insulation Heavy Build
[8]	Triple Insulated Wire: 25 AWG
[9]	Single core wire: 29 AWG (0.31 mm), insulation Single Build

WINDING INSTRUCTIONS

1. Primary - 1

Start with 1 lead(s) of Item [5] from Pin 3, use Item [3] at the start leads, and wind 51 turns in Clockwise direction in total of 2 layer(s). Wind one layer from left to right. Before each new layer, add 1 layer of tape, Item [6].At the end of 1st layer, continue to wind the next layer towards the beginning of the previous layer. Finish this winding on Pin 2, and use Item [3] at the finish leads. Add 1 layer(s) of tape, Item [6], on the top.

2. Primary Bias

Start with 4 lead(s) of Item [7] from Pin 4, use Item [3] at the start leads, bring the wire to the other side of the coil-former, and wind 10 turns in Clockwise direction in total of 1 layer(s). Wind one layer from right to left. Finish this winding on Pin 5, and use Item [3] at the finish leads. Add 1 layer(s) of tape, Item [6], on the top.

3. Secondary - 1 - 1

Start with 1 lead(s) of Item [8] from Pin 10, bring the wire to the other side of the coil-former, and wind 10 turns in Clockwise direction in total of 1 layer(s). Wind one layer from right to left. Finish this winding on Pin 9. Add 1 layer(s) of tape, Item [6], on the top.

4. Secondary - 1 - 2

Start with 1 lead(s) of Item [8] from Pin 10, bring the wire to the other side of the coil-former, and wind 10 turns in Clockwise direction in total of 1 layer(s). Wind one layer from right to left. Finish this winding on Pin 9. Add 1 layer(s) of tape, Item [6], on the top.

5. Secondary - 2

Start with 2 lead(s) of Item [9] from Pin 12, use Item [3] at the start leads, and wind 11 turns in Clockwise direction in total of 1 layer(s). Wind one layer from left to right. Finish this winding on Pin 11, and use Item [3] at the finish leads. Add 3 layer(s) of tape, Item [6], on the top.

6. Primary - 2

Start with 1 lead(s) of Item [5] from Pin 2, use Item [3] at the start leads, and wind 25 turns in Clockwise direction in total of 1 layer(s). Wind one layer from left to right. Spread the winding evenly across the entire bobbin. Finish this winding on Pin 1, and use Item [3] at the finish leads. Add 2 layer(s) of tape, Item [6], on the top.

BUILDING PREPARATIONS

1. Gap the core halves to get 1448 uH +- 5.0%.

FINISHING INSTRUCTIONS

1. Use a flux-band around the core connected to +DC may improve the EMI performance.
2. Varnish with Item [4]

ELECTRICAL PARAMETERS

Parameter	Condition	Spec
Electrical Strength	60 Hz 1 second, from pins 1,2,3,4,5 to pins 10,11,12,9.	3000 VAC
Nominal Primary Inductance	Measured at 1 V pk-pk, typical switching frequency, between pin 3 to pin 1, with all other Windings open.	1448 uH +- 5.0%
Maximum Primary Leakage	Measured between Pin 3 to Pin 1, with all other Windings shorted.	16.24 uH

Comments:

Achieving compliance to applicable safety standard may require additional considerations for transformer construction, manufacturing and methods used for termination of wires.
It is the responsibility of the user to verify that all applicable safety requirements are met and make additional changes as applicable.

Winding Parameters

Type	Power	Power	Power	Power	Bias	Power
Name	Primary - 2	Secondary - 2	Secondary - 1 - 2	Secondary - 1 - 1	Primary Bias	Primary - 1
Turns	25	11	10	10	10	51
Layers	1	0.96	1	1	0.96	2
Color	Red	Pink	Blue	Blue	Orange	Red
Wire Type	Single Core	Single Core	Single Core	Single Core	Single Core	Single Core
Wire Size, AWG	30	29	25	25	35	30
Wire Grade	Heavy Build	Single Build	TIW	TIW	Heavy Build	Heavy Build
Filar	1	2	1	1	4	1
Wire Tolerance, %	0	0	0	0	0	0
Split	Series	False	Parallel	Parallel	False	Series
Continuous Pin	None	-	-	-	-	None
Spread	YES	NO	NO	NO	NO	NO
Arrangement	Independent	Independent	Independent	Independent	Independent	Independent
Direction	Clockwise	Clockwise	Clockwise	Clockwise	Clockwise	Clockwise
Z winding	NO	NO	NO	NO	NO	NO
Opposite start	NO	NO	YES	YES	YES	NO
Winding Start	Pin	Pin	Pin	Pin	Pin	Pin
Winding End	Pin	Pin	Pin	Pin	Pin	Pin
Start Pin	2	12	10	10	4	3
End Pin	1	11	9	9	5	2
Sleeving	Sleeve Both	Sleeve Both	None	None	Sleeve Both	Sleeve Both
Connection	Split	Floating	Split	Split	Floating	Split
Margin Left	0	0	0	0	0	0
Margin Right	0	0	0	0	0	0
Tape Between Layers	YES	NO	NO	NO	NO	YES
Tape Between Lead & Winding	NO	NO	NO	NO	NO	NO
Tape on top	2	3	1	1	1	1
Tape Thickness, mm	0.0254	0.0254	0.0254	0.0254	0.0254	0.0254
CMA, Cmils/A	365.04	293.98	229.07	207.86	12501.71	365.04

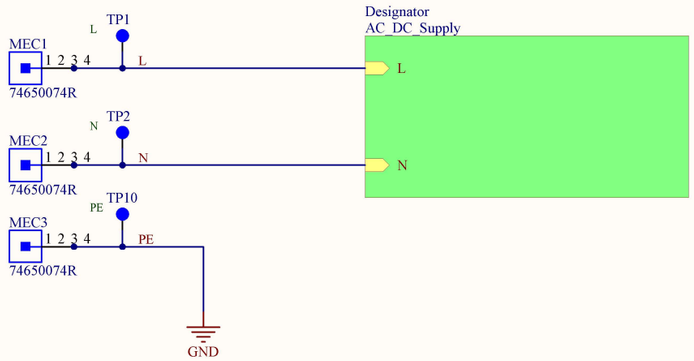
Core/Coil Former Parameters

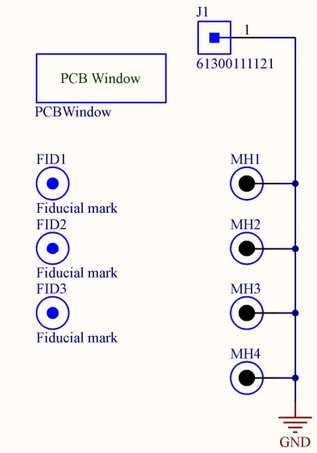
Core Type	PQ20 (PQ20/16-3F3)
Part Number	PQ20/16-3F3
Core Material	3F3
Coil Former Part Number	CPV-PQ20/16-1S-14P
Bobbin type	Vertical
Available Pins	14
BW, mm	7.82
BFW, mm	4.17
Bobbin Window Length, mm	7.82
X-Tolerance, %	0
Maximum Stack Height, mm	4.17
Y-Tolerance, %	0
External shielding	None
Core connect to	

Appendix B

Altium Designer outputs

This appendix includes the design outputs from Altium Designer software.





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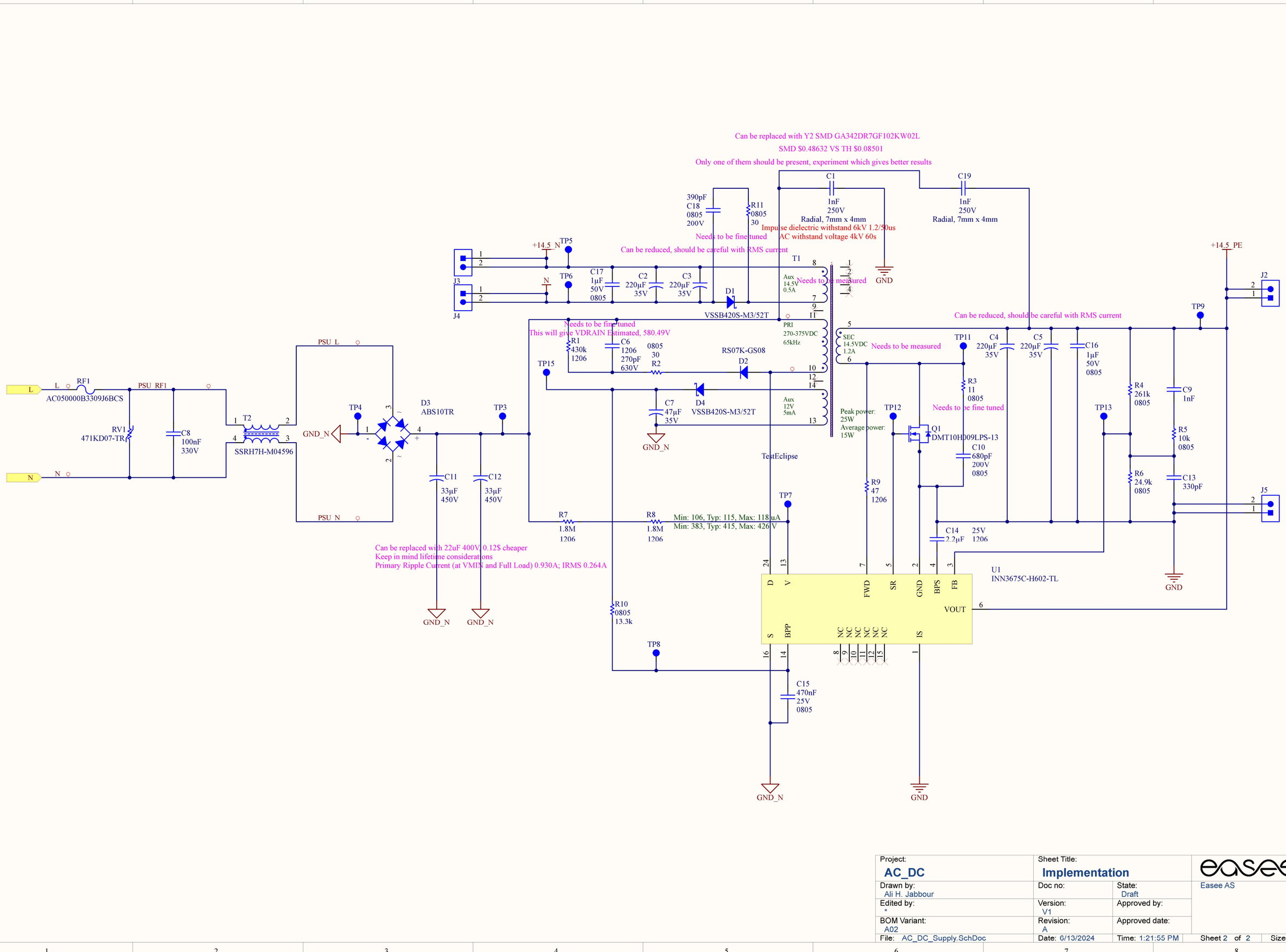
Edited by: *	Version: V1	Approved by:	
BOM Variant: A02	Revision: A	Approved date:	
File: TopView.SchDoc	Date: 6/13/2024	Time: 1:21:55 PM	Sheet 1 of 2 Size:A3



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Edited by: *	Version: V1	Approved by:	
BOM Variant: A02	Revision: A	Approved date:	
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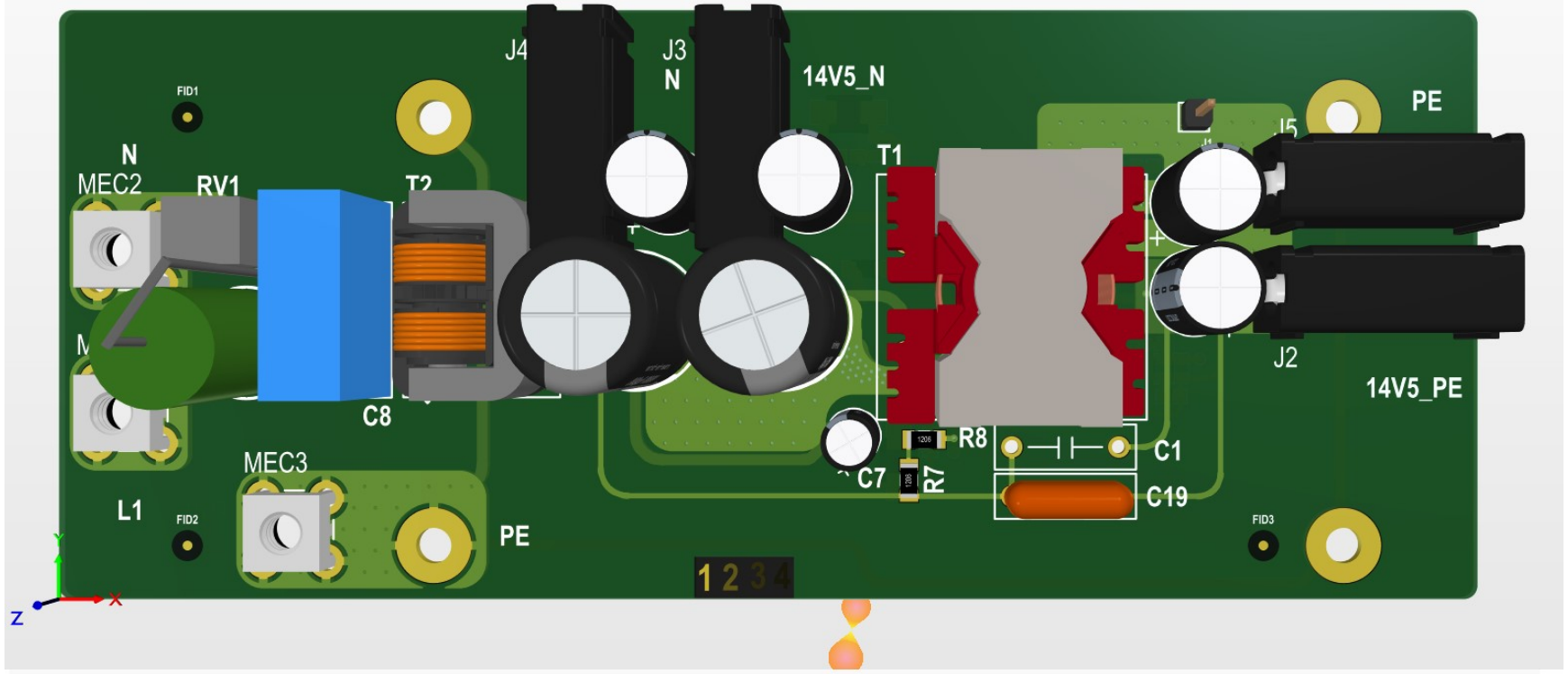
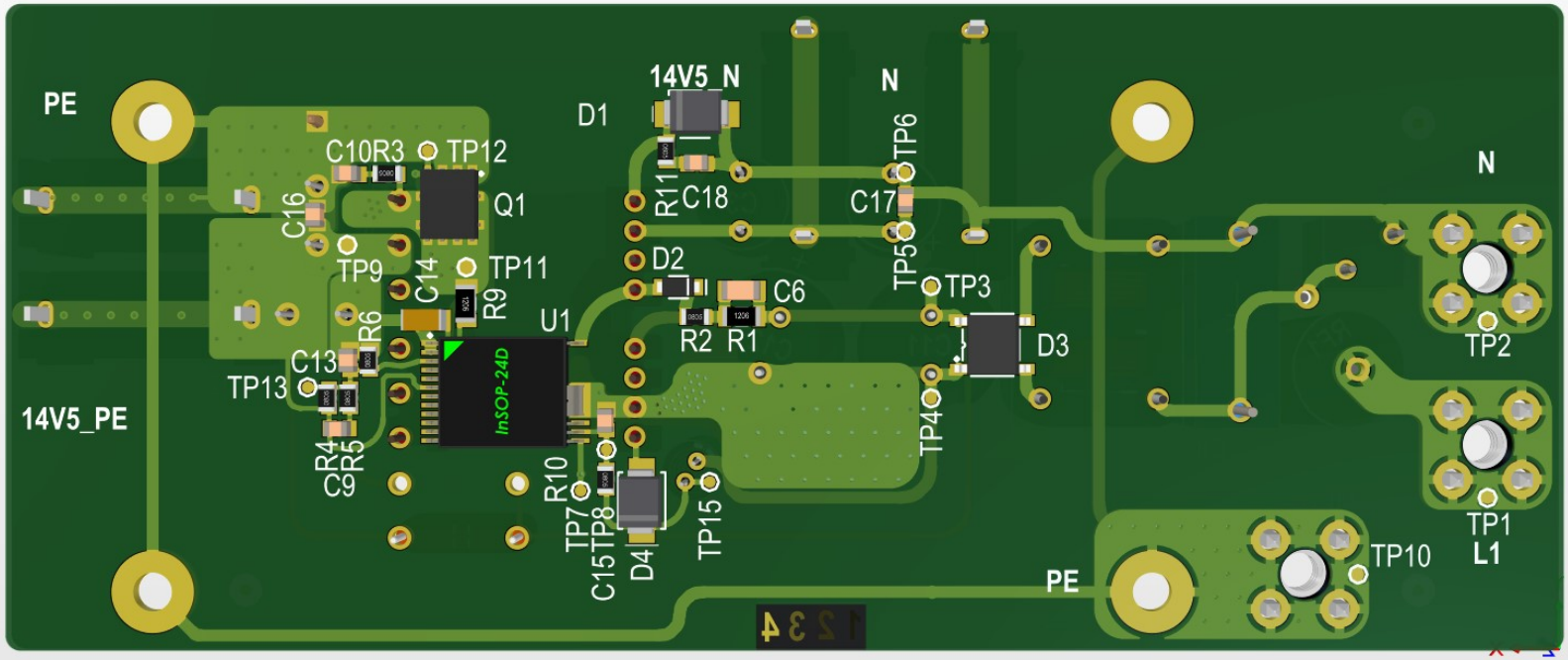
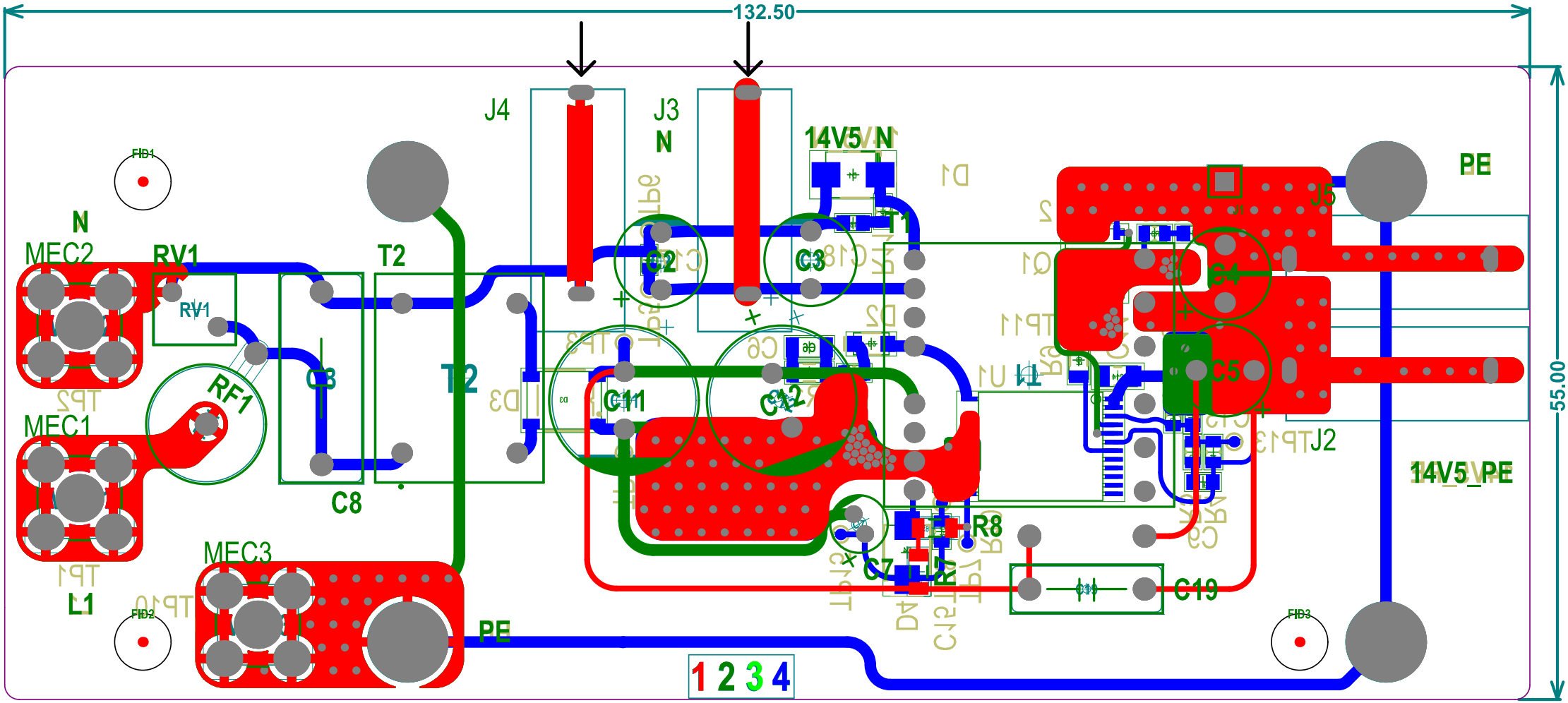
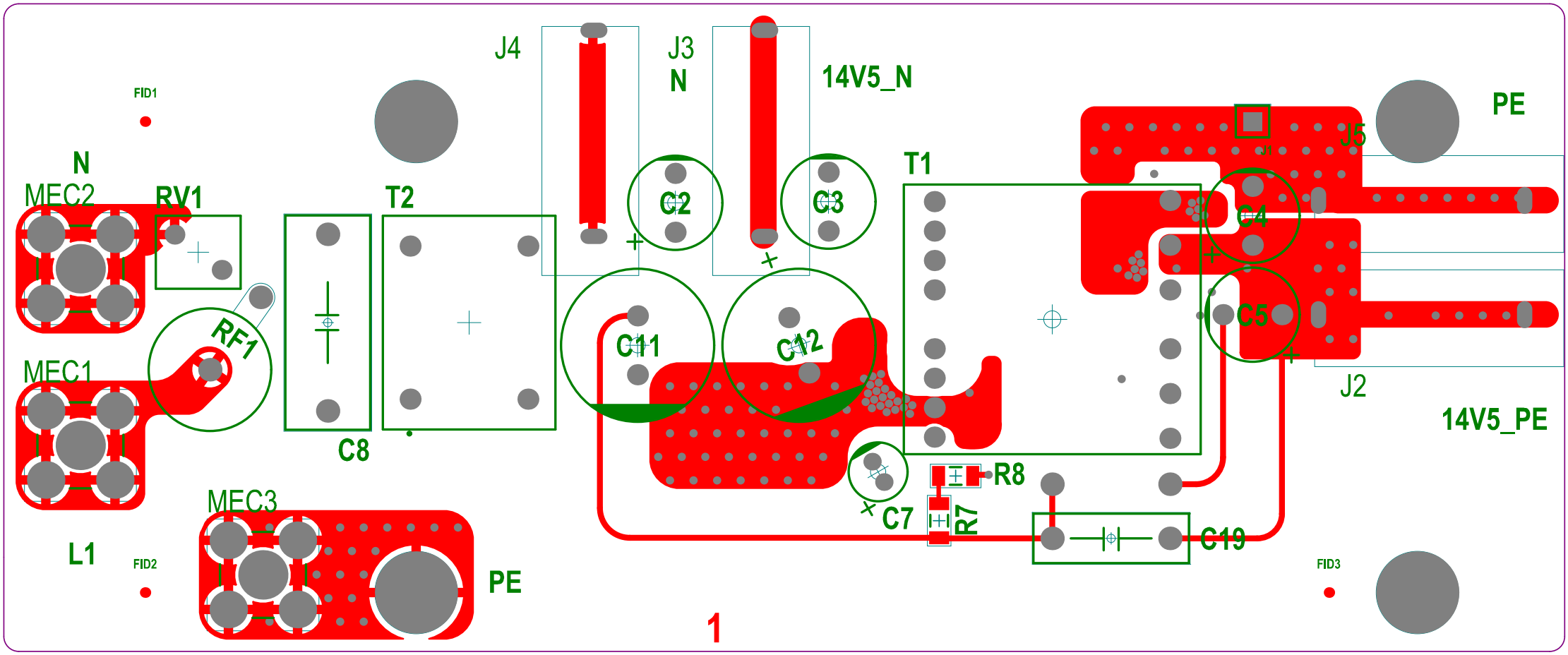

J4
J3
N
14V5_N
PE
FID1
N
MEC2
RV1
T2
T1
J5
J2
14V5_PE
C8
MEC3
C7
R7
R8
C1
C19
L1
FID2
PE
FID3
1 2 3 4


PE
14V5_N
N
D1
C10
R3
TP12
Q1
C16
TP9
C14
TP11
R9
U1
R6
C13
TP13
InSOP-24D
14V5_PE
R4
R5
C9
R10
TP7
TP8
C15
D4
TP15
R11
C18
D2
C6
R2
R1
C17
TP6
TP5
TP3
D3
TP4
N
TP2
TP1
L1
TP10
PE

AC_DC V1-A1-A02




J4
J3
N
14V5_N
FID1
N
MEC2
RV1
T2
T1
C2
C3
J5
PE
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C5
RF1
MEC1
C11
C12
J2
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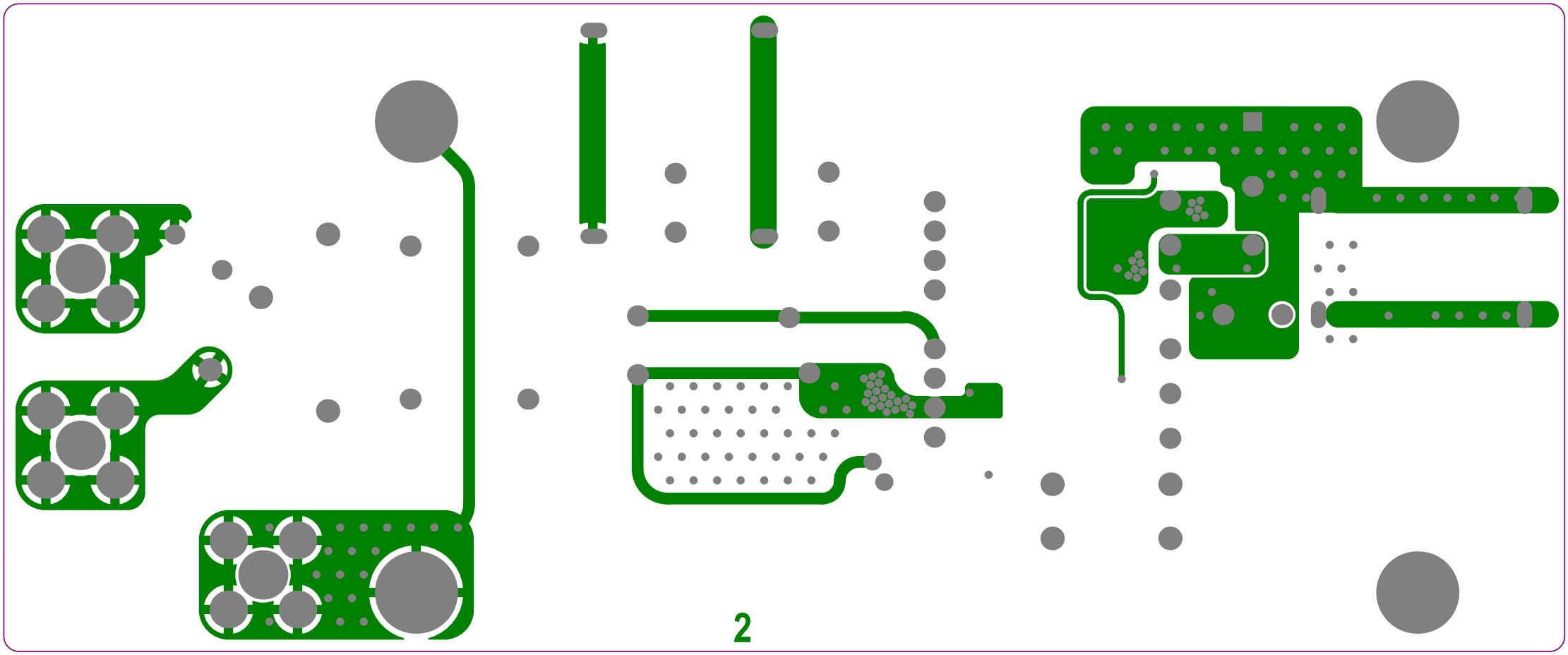
C8
MEC3
R8
C7
R7
C19
L1
FID2
PE
FID3
1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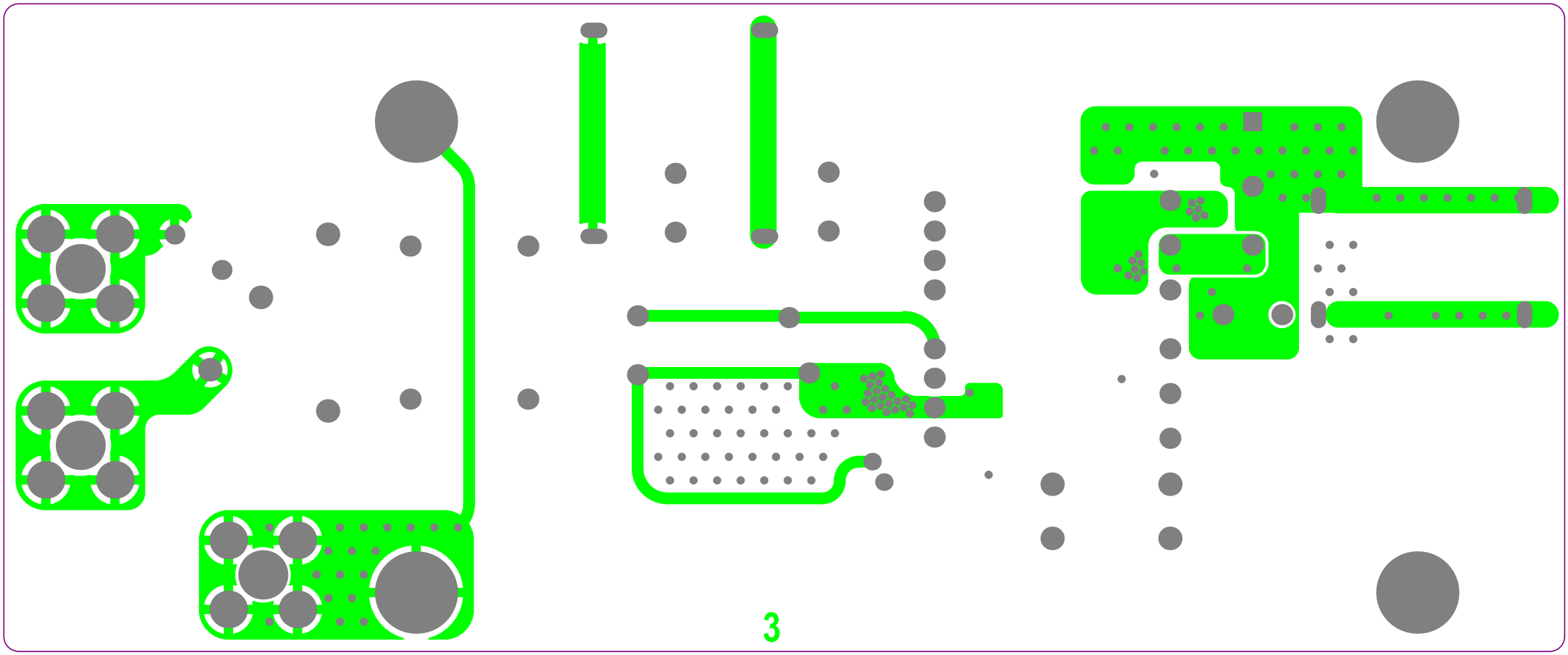
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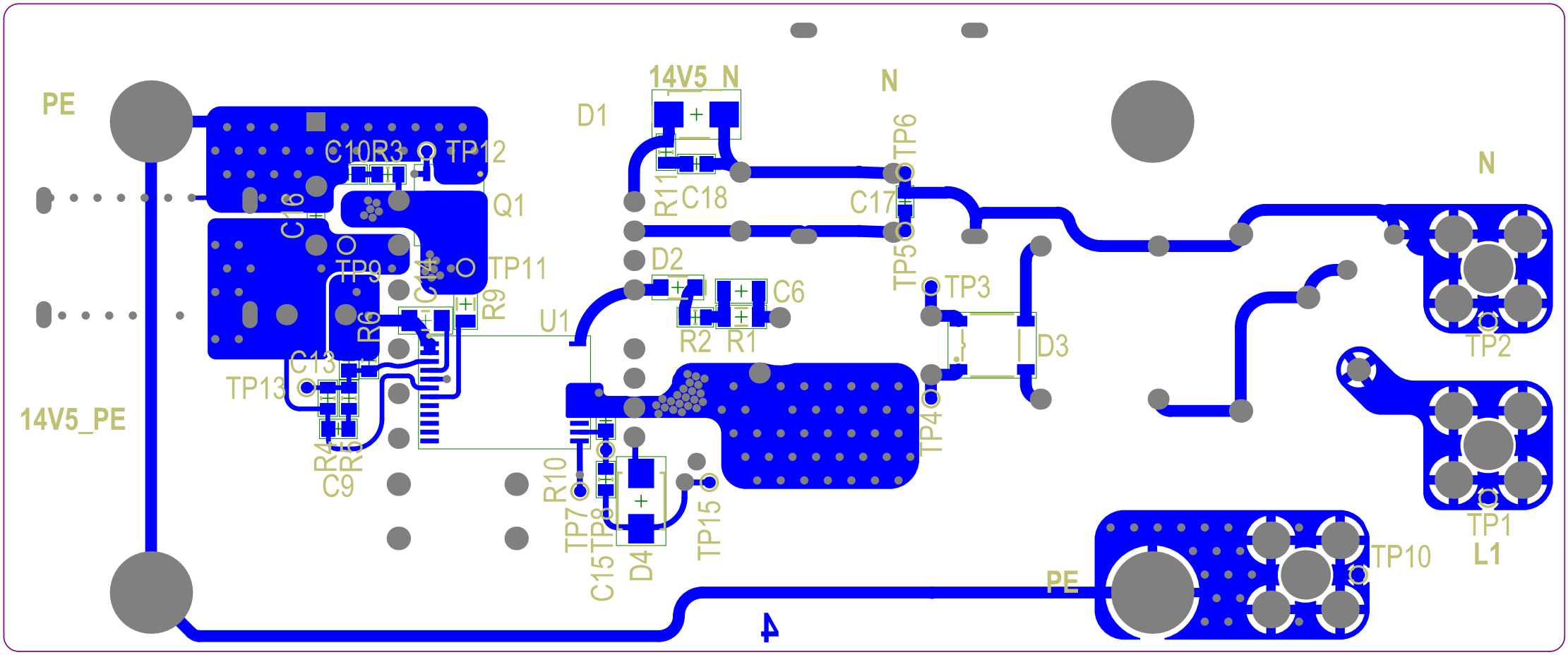
PE
14V5_N
N
D1
C10
R3
TP12
Q1
C16
TP9
TP11
C14
R9
R6
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TP13
14V5_PE
R4
R5
C9
R10
TP7
TP8
C15
D4
TP15
R11
C18
C17
TP6
TP5
D2
C6
R2
R1
TP3
D3
TP4
N
TP2
TP1
L1
TP10
PE

Item nr.	Name	Description	Designator	Quantity	Manufacturer	Manufacturer part nr.
1	35ZLH220MEFCTA8X11.5	Cap, Alu, 220uF, 35V, 20%, 8000h @ 105°C, Radial 8mm x 11.5mm, 5mm pitch	C2, C3, C4, C5	4	Rubycon	35ZLH220MEFC8X11.5
2	GRM31A5C2J271JW01D	Cap, Cer, 270pF, 630V, 5%, C0G/NP0, 1206	C6	1	Samsung	CL31C271JBCNNNC
3	35ZLH47MEFC5X11	Cap, Alu, 47uF, 35V, 20%, 6000h @ 105°C, Radial 5mm x 11mm, 2mm pitch	C7	1	Rubycon	35ZLH47MEFC5X11
4	B32912A3104K000	Cap, X1 safety, 100nF, 330VAC, 10%, Radial, 18mm x 7mm	C8	1	TDK EPCOS	B32912A3104K
5	Cap_std_0805_1nF	Cap, Cer, 1nF, 50V, 10%, X7R, 0805	C9	1	Samsung	CL21B102KBCNNNC
6	Cap_std_0805_680pF	Cap, Cer, 680pF, 200V, 10%, X7R, 0805	C10	1	Yageo	CC0805KRX7RABB681
7	450BXW33MEFR12.5X25	Cap, Alu, 33uF, 450V, 20%, 12000h @ 105°C, Radial 12.5mm x 25mm	C11, C12	2	Rubycon	450BXW33MEFR12.5X25
8	Cap_std_0805_330pF	Cap, Cer, 330pF, 50V, 10%, X7R, 0805	C13	1	Yageo	CC0805KRX7R9BB331
9	Cap_std_1206_2.2uF	Cap, Cer, 2.2uF, 25V, 10%, X7R, 1206	C14	1	Yageo	CC1206KKX7R8BB225
10	Cap_std_0805_470nF	Cap, Cer, 470nF, 25V, 20%, X7R, 0805	C15	1		
11	CL21B105KBFNNNG	Cap, Cer, 1uF, 50V, ±10%, X7R, 0805	C16, C17	2	Samsung	CL21B105KBFNNNG
12	Cap_std_0805_390pF	Cap, Cer, 390pF, 200V, 10%, X7R, 0805	C18	1	Yageo	CC0805KRX7RABB391
13	DE1E3RA102MN4AN01F	Cap, X1, Y1 safety, 1nF, 250VAC, 20%, Radial, 7mm x 4mm	C19	1	Murata	DE1E3RA102MN4AN01F
14	VSSB420S-M3/52T	Diode, Schottky, 200V, 4A,DO-214AA (SMB)	D1, D4	2	Vishay Semiconductors	VSSB420S-M3/52T
15	RS07K-GS08	Diode, Fast Rectifier, 800V, 500mA, DO-219AB-SMF	D2	1	Vishay Semiconductors	RS07K-GS08
16	ABS10TR	Diode, Standard Bridge Rectifier, 1000V, 0.5A, ABS (4pins)	D3	1	Diodes	ABS10A-13
17	61300111121	Conn, Header, TH, 1 Pos, 1 Row, 2.54mm Pitch, Straight	J1	1	Wurth Electronics	61300111121
18	973582100	Bananaplug connector, 1 pin	J2, J3, J4, J5	4	Altech	973582100
19	74650074R	Conn, Header, THT, 1 Pos, Straight, 7.0mm x 7.0mm	MEC1, MEC2, MEC3	3		
20	DMT10H009LPS-13	Transistor, MOSFET N-Channel, 1.3W, PowerDI5060-8	Q1	1	Diodes	DMT10H009LPS-13
21	Res_std_1206_430k	Res, SMD, 430k, 200V, 1%, 1/4W, 1206 (3216)	R1	1	Yageo	RC1206FR-07430KL
22	Res_std_0805_30R_0.5W	Res, SMD, 30R, 400V, 5%, 1/2W, 0805 (2012)	R2, R11	2		
23	Res_std_0805_11R_0.5W	Res, SMD, 11R, 400V, 5%, 1/2W, 0805 (2012)	R3	1		
24	Res_std_0805_261k	Res, SMD, 261kOhm, 150V, 1%, 1/8W, 0805	R4	1	Yageo	RC0805FR-07261KL
25	Res_std_0805_10k	Res, SMD, 10k Ohm, 150V, 1%, 1/8W, 0805	R5	1	Vishay	CRCW080510K0FKEA
26	Res_std_0805_24.9k	Res, SMD, 24.9kOhm, 150V, 1%, 1/8W, 0805	R6	1	Yageo	RC0805FR-0724K9L
27	Res_std_1206_1.8M	Res, SMD, 1.8M, 200V, 1%, 1/4W, 1206 (3216)	R7, R8	2	Yageo	RC1206FR-071M8L
28	Res_std_1206_47R	Res, SMD, 47R, 200V, 1%, 1/4W, 1206 (3216)	R9	1	Yageo	RC1206FR-0747RL
29	Res_std_0805_13.3k	Res, SMD, 13.3k, 150V, 1%, 1/8W, 0805 (2012)	R10	1	Yageo	RC0805FR-0713K3L
30	AC050000B3309J6BCS	Fuse, Fusible Resistor, 33Ohm , 5W, THT, Axial	RF1	1	Vishay BCcomponents	AC050000B3309J6BCS
31	471KD07-TR	Varistor, 470V, 29J, 1.2kA, Disc 7mm	RV1	1	Yageo	471KD07
32	TestEclipse	Transformer, 2 Aux, 1 Sec, 4kV AC isolation	T1	1		
33	SSRH7H-M04596	Common Mode Choke, 59.6mH, 400mA, , Ferrite, 18.0mm x 14.5mm	T2	1	KEMET	SSRH7H-M04596
34	INN3675C-H602-TL	Power Regulator, Flyback, 725V, 30W, InSOP-24D	U1	1	Power Integrations	INN3675C-H602-TL